Project No. 1
Multiplexer
ECE 485

Peter Chinetti

September 25, 2013

Date Performed: September 29, 2013
Instructor: Professor Borkar

1 Background

A multiplexer, or 'MUX' switches between multiple inputs based on a select signal. Digital multiplexers have significant application in digital hardware and processors. The specific device specified in the project is a multiplexer that switches seven bunches of five data lines.

2 Design

The design is simple. Select an input according to the select signal and forward that input to the output. A diagram of the specific mux (with the groupings of inputs/outputs and three select lines) can be found in block.png.

3 Implementation Details

The problem asked for the multiplexer to be built in two different ways: Behavioral and Structural.
From Ashenden's *VHDL Tutorial*, a behavioral design 'includes only process statements, which are collections of actions to be executed in sequence. These actions are called sequential statements and are much like the kinds of statements we see in a conventional programming language.' The behavioral model for the multiplexer was originally designed off of Ashenden's reference as well as http://www.cs.uregina.ca/Links/class-info/301/multiplexer/lecture.html, specifically the CASE statement description. Difficulty was encountered when trying to use a vector as output, so outputs were specified as individual bits, selected out of the input vectors.
The test bench was originally designed for the behavioral model, then retrofitted

to the structural model.
After some consultation with a former member of the class, I found a better way to implement the behavioral model. I replaced the bitwise output with a vector and generally cleaned up the design, removing a vestigial enable input.

In contrast, a structural model requires the design of subsystems, then the linking to form a larger whole. I could not readily find material on the Internet quickly detailing how to write a structural VHDL program. The former student again helped me, this time to understand how structural models were implemented.
For further technical detail on each of the two designs, look to the inline comments in the source.

4 Testing

4.1 Behavioral

A screenshot of the wave output from the behavioral design can be found in the included file 'behavioral.png'. In that wave plot, a, b ... g are the ordered sets of inputs, and q is the output. Sel is the selector, so as it changes you can track the output changing to the appropriate input.

4.2 Structural

A screenshot of the wave output from the structural design can be found in the included file 'structural.png'. In that wave plot i0, i1 ... i6 are the ordered sets of inputs, and output is the output. Sel remains the selector. Again, you can watch the mux switch to the appropriate input-output couple.