HW #4
ECE 446

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1

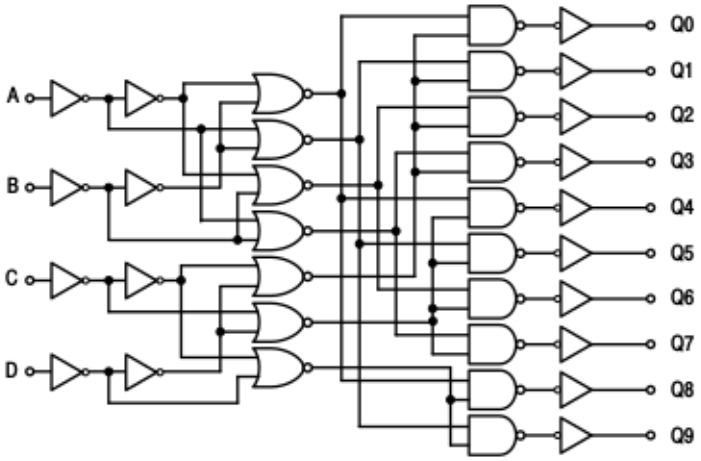
The longest delay is the path through all CO inputs through to all C4 outputs when switching high to low, for a total time of 22*4 = 88 ns.

2

		Output Delay							
Input	Direction	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
A	HL					41	41		
B	LH						20		20
C	HL		41				41		
G1	HL						38		
G2A	LH						18		
G2B	LH						18		

3

Looking at a professionally built decoder (MC14028B) schematic: you can use NOR gates to allow for only two input gating rather than 4 input.



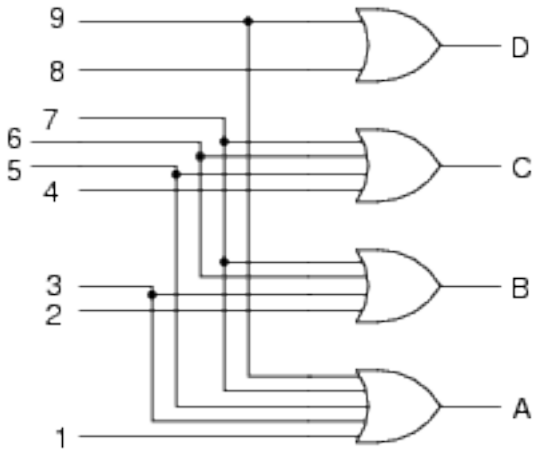
LOGIC DIAGRAM

4

It is an decoder. The top three inputs on the left side are the three decoder inputs. Below is the enable signals, the two complemented inputs to the left most AND gate are the two enable low signals, the uncomplemented input to the AND gate is the enable high signal. Below that is a selector of whether to have the outputs be active low or high. If that input is high, the outputs are active high, otherwise they are active low. On the right side, the top 8 outputs are the decoded outputs, the bottom output is an active low enable chain output.

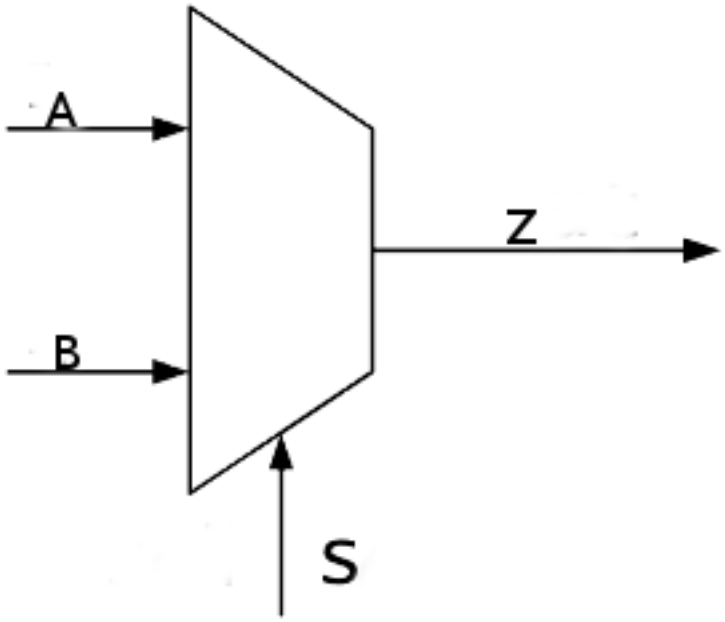
5

Using only OR gates:



6

A	B	S	Z
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

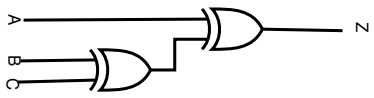


7

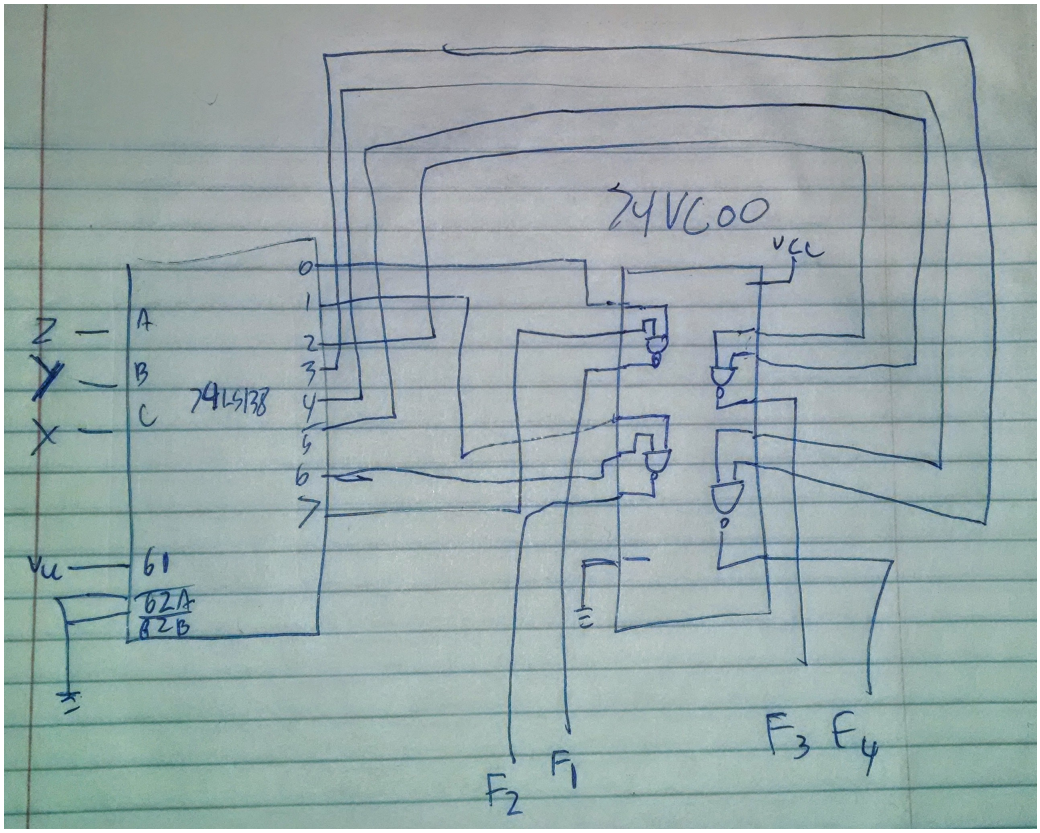
XNOR

8

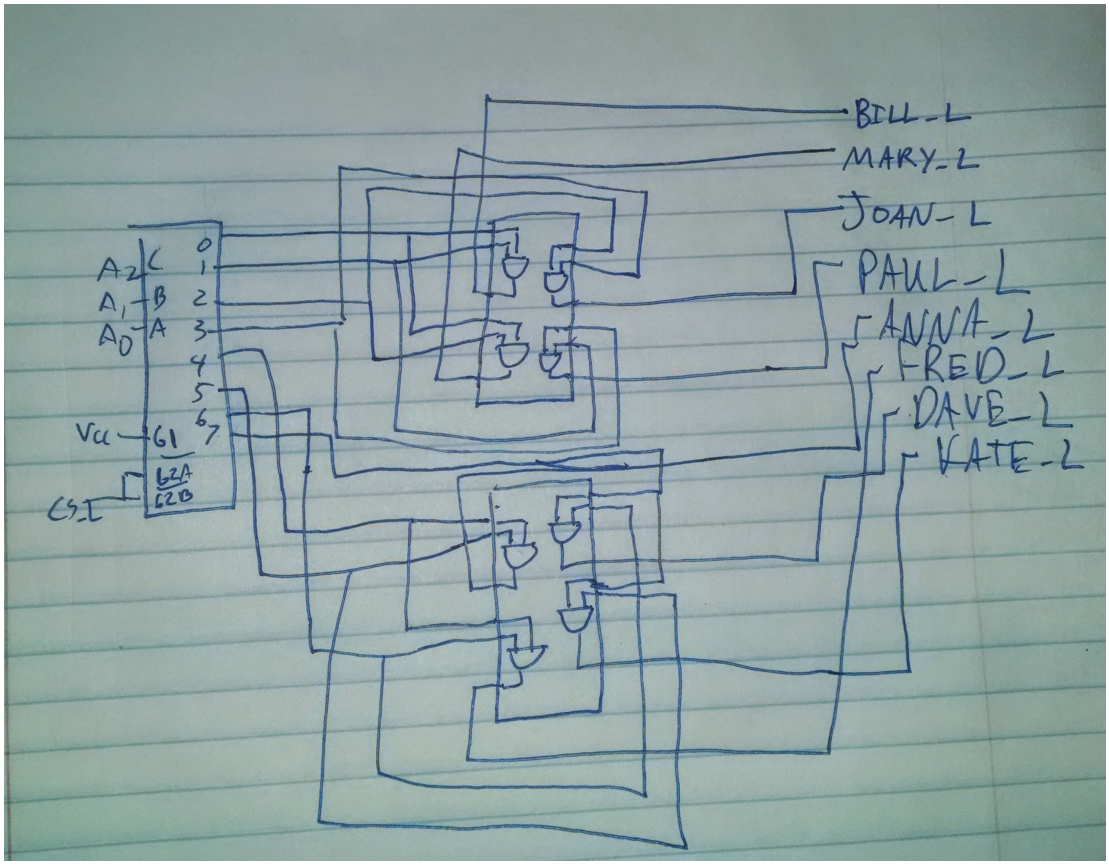
A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



9



10



11

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity min_max is
  Port ( X : in  STD_LOGIC_VECTOR( 7 downto 0);
         Y : in  STD_LOGIC_VECTOR( 7 downto 0);
         MIN_MAX : in STD_LOGIC;
         Z : out STD_LOGIC_VECTOR( 7 downto 0));
end min_max;

architecture arch of min_max is
begin
  process (X,Y,MIN_MAX)
  begin
```

```
    if (X(0) xnor Y(0)) and (X(1) xnor Y(1)) and (X(2) xnor Y(2))
    and (X(3) xnor Y(3)) and (X(4) xnor Y(4)) and (X(5) xnor Y(5))
    and (X(6) xnor Y(6)) and (X(7) xnor Y(7)) then
      Z <= "00000000";

    elsif ((X(0) and not Y(0))) or ((X(0) xnor Y(0)) and (X(1) and
    not Y(1))) or ((X(0) xnor Y(0)) and (X(1) xnor Y(1)) and (X(2)
    and not Y(2))) or ((X(0) xnor Y(0)) and (X(1) xnor Y(1)) and (X
    (2) xnor Y(2)) and (X(3) and not Y(3))) or ((X(0) xnor Y(0))
    and (X(1) xnor Y(1)) and (X(2) xnor Y(2)) and (X(3) xnor Y(3))
    and (X(4) and not Y(4))) or ((X(0) xnor Y(0)) and (X(1) xnor Y
    (1)) and (X(2) xnor Y(2)) and (X(3) xnor Y(3)) and (X(4) xnor Y
    (4)) and (X(5) and not Y(5))) or ((X(0) xnor Y(0)) and (X(1)
    xnor Y(1)) and (X(2) xnor Y(2)) and (X(3) xnor Y(3)) and (X(4)
    xnor Y(4)) and (X(5) xnor Y(5)) and (X(6) and not Y(6))) or ((X
    (0) xnor Y(0)) and (X(1) xnor Y(1)) and (X(2) xnor Y(2)) and (X
    (3) xnor Y(3)) and (X(4) xnor Y(4)) and (X(5) xnor Y(5)) and (X
    (6) xnor Y(6)) and (X(7) and not Y(7))) then
      if MIN_MAX = '1' then
        Z <= Y;
      else
        Z <= X;
      end if;
    else
      if MIN_MAX = '1' then
        Z <= X;
      else
        Z <= Y;
      end if;
    end if;
  end process;

end arch;
```

11.vhd