HW #3
ECE 446

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1

1.1 HL

Gate	1	2	3	4	5	6
Transition	HL	LH	HL	LH	HL	LH
Delay [ns]	15	15	15	15	15	15
Total [ns]	90					

1.2 LH

Gate	1	2	3	4	5	6
Transition	LH	HL	LH	HL	LH	HL
Delay [ns]	15	15	15	15	15	15
Total [ns]	90					

1.3 Worst Case Delay

Gate	1	2	3	4	5	6
Worst Case Delay [ns]	15	15	15	15	15	15
Total [ns]	90					

1.4 Discussion

Because the delays are symmetrical, there is no difference between the worst case and the actual performance of the chips.

2

2.1 HL

Gate	1	2	3	4	5	6
Transition	HL	LH	HL	LH	HL	LH
Delay [ns]	20	15	20	15	20	15
Total [ns]	105					

2.2 LH

Gate	1	2	3	4	5	6
Transition	LH	HL	LH	HL	LH	HL
Delay [ns]	15	20	15	20	15	20
Total [ns]	105					

2.3 Worst Case Delay

Gate	1	2	3	4	5	6
Worst Case Delay [ns]	20	20	20	20	20	20
Total [ns]	120					

2.4 Discussion

Because the delays are not symmetrical, there is a difference between the worst case and the actual performance of the chips.

3

3.1 HL

Gate	1	2	3	4
Transition	LH	LH	LH	HL
Delay [ns]	23	23	23	17
Total [ns]	86			

3.2 LH

Gate	1	2	3	4
Transition	HL	HL	HL	LH

Delay [ns]	17	17	17	23
Total [ns]	74			

3.3 Worst Case Delay

Gate	1	2	3	4
Worst Case Delay [ns]	23	23	23	23
Total [ns]	92			

3.4 Discussion

Because the delays are not symmetrical, there is a difference between the worst case and the actual performance of the chips.

4

4.1 74LS138

The longest delay through the 74LS138 is from any select line to the 2^{nd} output, with a delay of 41ns.

4.2 74LS139

The longest delay through the 74LS139 is from any select line to the 3^{rd} output, with a delay of 38ns.

4.3 Total Delay

Although the the longest delay is through the select lines, the longest delay in the circuit is through the select to the output 3 on the 74LS139 then through the G2B to the output, with a total time of 70ns.