Exam No. 1
ECE 446

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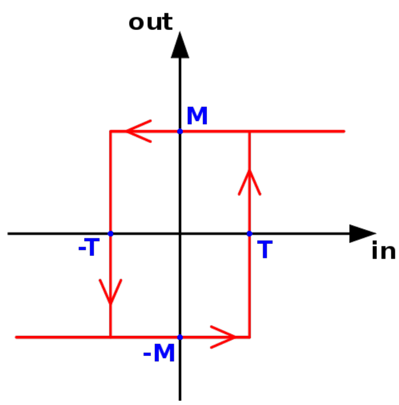
1.A

A Schmitt trigger has two input trigger voltages, low and high and two output rails. When the output of the Schmitt trigger is at one of the rails, the input must pass the opposite trigger voltage before the output switches to the other rail. Therefore, the output is dependent on both the input and the past states the trigger. Dependence on inputs and past states is called Hysteresis. A pictorial representation of the input and output of the trigger is below.

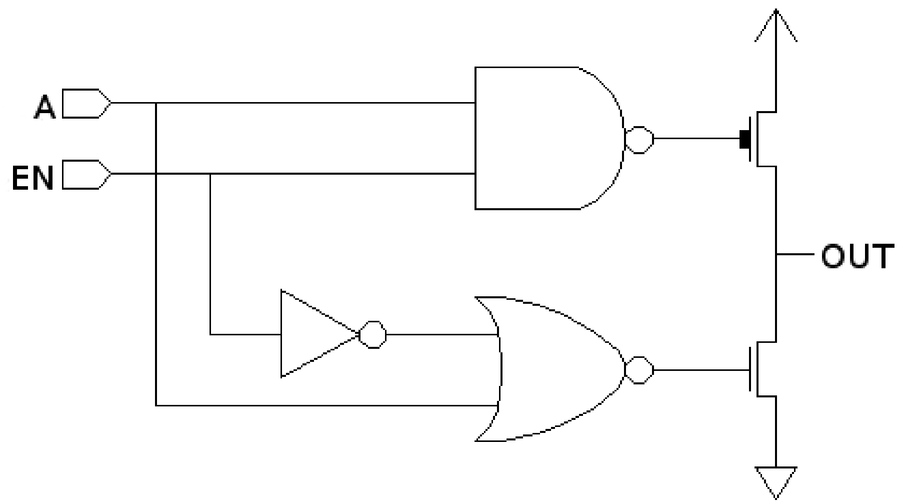


In that diagram, M/-M are the rail voltages, and T/-T are the trigger voltages.

1.B

Three state buffers allow a gate to be driven high, low, or disabled and in a ‘High-Z’ state. The High-Z state is a high impedance state that allows the gate to be externally driven (such as in a bus) without burning the drive transistors.

1.C



1.D

$D \cdot \overline{B} + \overline{D} \cdot B$

2

2.A

A static hazard occurs when one input variable changes, and the output changes momentarily before stabilizing to the correct value.
The Static-1 Hazard covers the situation where the outputs momentarily blip from 1 to 0 as the inputs change. The Static-0 Hazard covers the opposite.

2.B

Yes.
When Y transitions from 1 to 0 when X and Z are 1, the will be a momentary delay as the XY and gate drops before the not gate and the $\overline{Y}Z$ and gate transitions.
To fix the hazard, include a redundant miniterm. $F = X \cdot Y + X \cdot \overline{Z} + \overline{Y} \cdot Z$.

2.C

Yes.
There is a Static-0 hazard, if the gates are $X = 0, Z = 0$, and Y transitions from 0 to 1. The delay in the NOT gate introduces a delay on switching the

bottom OR gate, Which causes a momentary transition on the output.
To fix the hazard, include a redundant maxterm. $F = (X+Y)\cdot(X+Z)\cdot(\overline{Y}+Z)$

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3.A

AB\CD	00	01	11	10
00	0	1	0	1
01	1	0	1	0
11	0	1	0	1
10	1	0	1	0

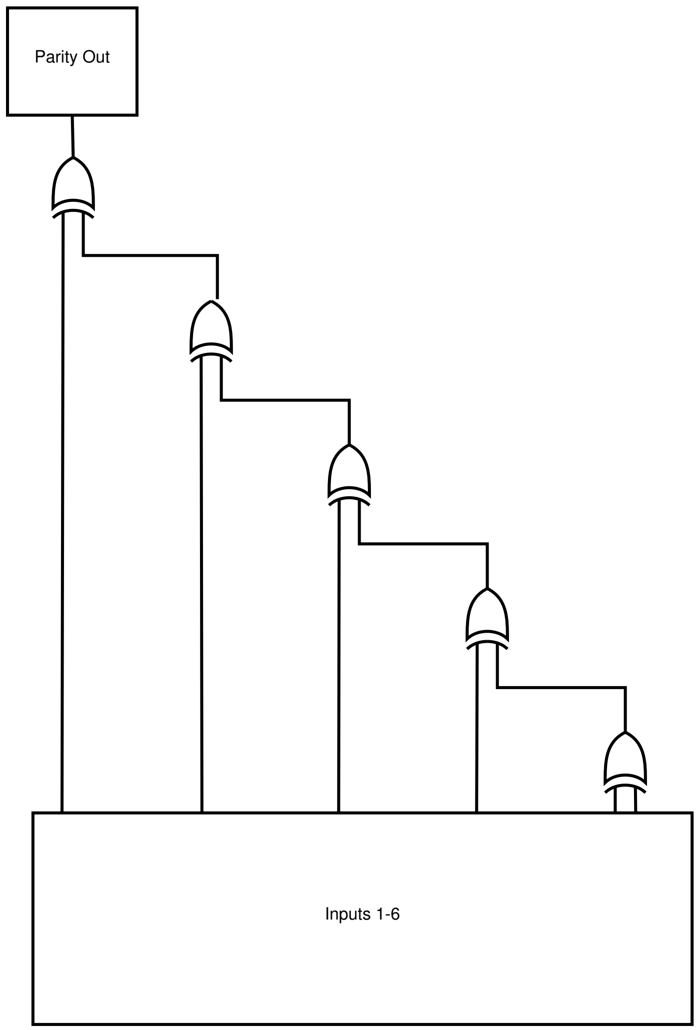
3.B

2^{n-1}, half the permutations.

3.C

2^{n-1}, they don't minimize.

3.D



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4.A T

4.B T

4.C F

4.D F

4.E F

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5.A

$F = Z + X \cdot \overline{Y} \cdot \overline{Z}$
$F' = (Z + X \cdot \overline{Y} \cdot \overline{Z})'$
$= (\overline{Z}) \cdot (\overline{X} + Y + Z)$
$= \overline{Z} \cdot \overline{X} + \overline{Z} \cdot Y + \overline{Z} \cdot Z$
$= \overline{Z} \cdot \overline{X} + \overline{Z} \cdot Y$
$(F')' = (\overline{Z} \cdot \overline{X} + \overline{Z} \cdot Y)'$
$= (Z + X) \cdot (Z + \overline{Y})$

5.B

$F' = (XY + XZ + YZ')'$
$= (\overline{X} + \overline{Y})(\overline{X} + \overline{Z})(\overline{Y} + Z)$
$= (\overline{XX} + \overline{YX} + \overline{XZ} + \overline{YX})(\overline{Y} + Z)$
$= (\overline{X} + \overline{YX} + \overline{XZ} + \overline{YX})(\overline{Y} + Z)$
$= \overline{XY} + \overline{YYX} + \overline{YXZ} + \overline{YYZ} + Z\overline{X} + Z\overline{YX} + Z\overline{XZ} + Z\overline{YZ}$
$= \overline{XY} + \overline{YX} + \overline{YXZ} + \overline{YZ} + Z\overline{X} + Z\overline{YX}$
$= \overline{XY} + \overline{YXZ} + \overline{YZ} + Z\overline{XY} + Z\overline{X}$
$= \overline{XY}Z + \overline{XYZ} + X\overline{YZ} + ZY\overline{X}$
$= X\overline{YZ} + \overline{X}YZ + \overline{XY}Z + \overline{XYZ}$
$(F')' = F = (\overline{X} + Y + Z)(X + \overline{Y} + \overline{Z})(X + Y + \overline{Z})(Z + Y + Z)$

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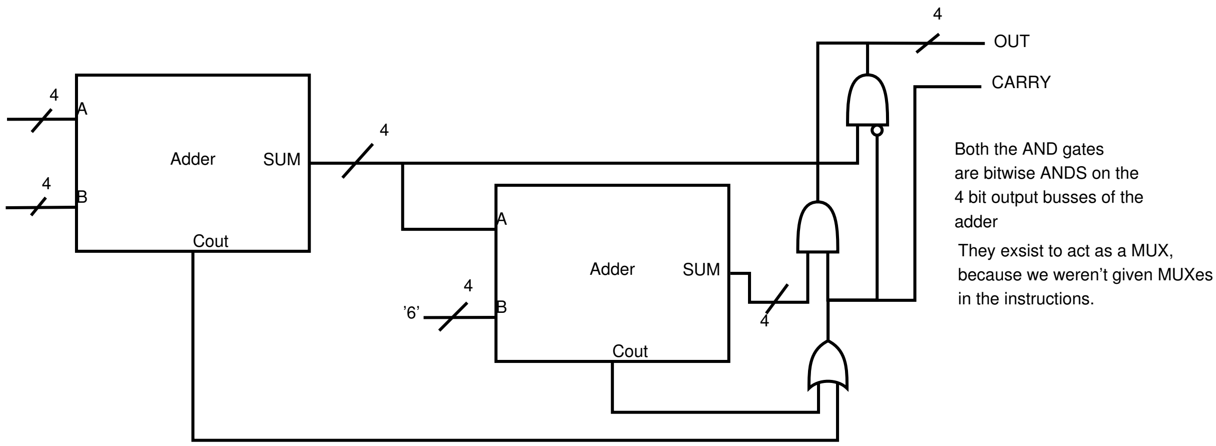
6.A



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7.A

Note: $\overline{\oplus}$ is the XNOR symbol

7.A.1 $A = B$

$(A0\overline{\oplus}B0)\cdot(A1\overline{\oplus}B1)\cdot(A2\overline{\oplus}B2)\cdot(A3\overline{\oplus}B3)$

7.A.2 $A > B$

$A3\cdot\overline{B3}+(A3\overline{\oplus}B3)\cdot A2\cdot\overline{B2}+(A3\overline{\oplus}B3)\cdot(A2\overline{\oplus}B2)\cdot A1\cdot\overline{B1}+(A3\overline{\oplus}B3)\cdot(A2\overline{\oplus}B2)\cdot(A1\overline{\oplus}B1)\cdot A0\cdot\overline{B0}$

7.A.3 $A < B$

$(\overline{A = B})\cdot(\overline{A > B})$

7.A.4 AGTBOUT

$(A > B) + (A = B)\cdot(AGTBIN)$

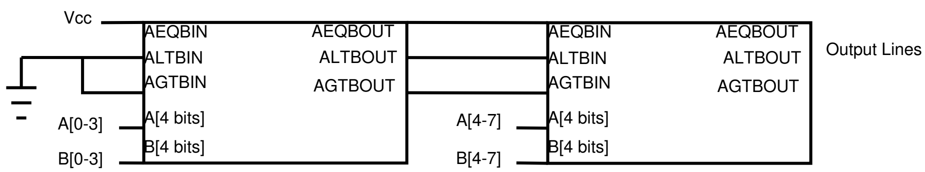
7.A.5 ALTBOUT

$(A < B) + (A = B)\cdot(ALTBIN)$

7.A.6 AEQBOUT

$(A = B) \cdot (AEQBIN)$

7.B



7.C

7.C.1

$\overline{AEQBOUT_{high}}$

7.C.2

$AEQBOUT_{high} + AGTBOUT_{high}$

7.C.3

$AEQBOUT_{high} + ALTBOUT_{high}$

8

8.A

To send 16 bits in a hamming code, 21 bits must be transmitted formatted as follows:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
P1	P2	D1	P3	D2	D3	D4	P4	D5	D6	D7	D8	D9	D10	D11	P5	D12	D13	D14	D15	D16

Where the top row is bit position and the bottom is the use of the bit. P bits are parity bits, and D bits are data bits. the P bits are generated through these algorithms:
P1 = xor of bits with 1's place bit set.
P2 = xor of bits with 2's place bit set.
P3 = xor of bits with 4's place bit set.
P4 = xor of bits with 8's place bit set.
P5 = xor of bits with 16's place bit set.

8.B

After receving a hamming code encoded signal, check bits are generated by XORing the parity bits with the bits that originally generated them. If the check bits are nonzero, an error occured in transit. If that is the case, the check bits will read out the bit position at which the error occured. This bit can be flipped and the single bit error corrected.