ECE 446 – Advanced Logic Design & Implementation

Course Policies and Syllabus

Fall 2014

Instructor

Professor Jafar Saniie
Office: 103 Siegel Hall
Office Hours: Monday and Wednesday 12:45 PM – 1:30 PM

Lectures: Monday 5:00 PM – 7:40 PM

Course Objectives

This course will provide the background needed to design digital systems at a professional level. Students learn about the design principles and practices. Through the entire course student use VHDL to design and implement both combinational and sequential logic devices. In particular, students will learn the design of many widely used MSI combinational and sequential devices. Topics will include capabilities and limitations of digital logic families, conservative practices for the design of large digital systems, and advanced logic design techniques. Classroom instruction will be complemented by four orientation laboratories and eight design-oriented lab projects.

Prerequisites: ECE 218, ECE 214, ECE 311, and senior standing.

Grading

- Midterm Exam 30% (October 20, 2014, 5:00PM – 7:30 PM)
- Final Exam 40% (December 8, 2014, 5:00 PM – 7:00 PM)
- Homework 5%
- Laboratory 25%

Textbooks and Laboratory Manual

1. J. Wakerly, *Digital Design, Principles and Practices*, Prentice Hall, 3rd. Ed., 2000.
2. ECE 446 Laboratory Manual.

References

1. Texas Instruments, *The TTL Data Book.*
2. R. Katz, *Contemporary Logic Design*, Benjamin-Cummings, 1994.
3. M. Mano, Digital Design, Prentice Hall.
4. Additional references and course notes will be provided throughout the course.

Holidays

Labor Day (September 1), Fall Break (October 13), Thanksgiving (November 26-28)

Note

Labs begin August 26. NO LABS on September 2, 3 and 5.

Course Material

Download at http://ephesus.ece.iit.edu/~tgonnot/ECE446-F14.zip, password is: ***ECE446-F14-ZIP***

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Course Syllabus

1. **Introduction to Digital Design, Number Systems and Codes, Survey Logic Design Technology (chip packaging and manufacturing), Overview of Logic Design Laboratory Assignments, Discussion of Orientation Laboratories, VHDL Programming and FPGAs (6 Classes)**

2. **Boolean Algebra, Combinational Circuits, Karnaugh Maps, Logic Minimization, Discussion of Error Correcting Codes Laboratory, Combinational Circuit Analysis and Synthesis, Schematics and Documentation Standards (6 Classes)**

3. **Discussion on the Operation of the Logic Analyzer, Combinational Logic Delay, Hazard Detection and Correction (3 classes)**

4. **Design of Parity Generators and Checkers, Comparators, Encoders and Decoders, and Arithmetic Circuits (ripple adder, carry lookahead adders, subtractor and multipliers), transmission gates, Schmitt Trigger Inputs, Three-State Outputs, Open-Drain Outputs, Wired Logic, Multiplexers, Demultiplexers, Buses, Building Block Designs, Barrel Shifter, Simple Floating Point Encoder, Mode-Dependent Comparators, Design of D/A and A/D Converters, Design Examples Using VHDLs (15 classes).**

5. **Sequential Logic Design Principles: S-R Latch with Enable, D Latch, Edge-Triggered D Flip/Flops, Scan Flip/Flops, Edge-Triggered J-K flip/flops, T Flip/Flops, Switch Debouncer, Mealy and Moore Machines, State Machine Analysis, and State Machine Synthesis Using D, J-K, and T Flip/Flops, Algorithmic State Machine (ASM), Design of Latches, Shift Registers, Counters, Serial-to-Parallel and Parallel-to-Serial Converters, Sequential Logic Design Examples (9 Classes)**

6. **Synchronous Design Methodology, Synchronizer Failure and Metastability, Dynamic Electrical Behavior (Propagation Delay and Power Consumption), Noise Margin and Fanout (3 classes)**

7. **Tests (3 classes)**

Laboratory Assignments and Projects:

Table of Contents

Week	Lab Number	Name	Notes
Week 1	**Combinational VHDL**	• **Introduction to VHDL** • **Using ISE and ISIM**	**Tutorial**
	Lab 1	**Code Conversion**	
Week 3	**Lab 2**	**Four-Bit Ripple-Carry Adder/Subtractor**	**Make-up Lab**
	Lab 3	**Hazards and Glitches**	
Week 4	**Lab 4**	**Error Correcting Codes**	
Week 5	**Lab 5**	**Barrel Shifters**	
Week 6	**Lab 6**	**High-Speed Adder/Subtractor**	
Week 7	**Sequential VHDL**	• **Finite State Machine** • **Using StateCAD**	**Tutorial**
Week 8	**Lab 7**	**Sequential Logic Design and Finite State Machines (StateCAD)**	**Make-up Lab**
Week 9	**Lab 8**	**Traffic Light Controller**	
Week 10	**Lab 9**	**Data Encryption Using LFSRs**	
Week 11	**Lab 10 & 11**	**D/A and A/D Converters**	
Week 12	**Lab 12**	**Successive Approximation A/D Converter**	
Week 13-14	**Project**	**Serial Data Transmitter – Receiver**	**Make-up Labs**

Archive Content

Some folders contain "readme.txt ". Please read these files before continue.
The archive will be available at the following address:
http://ephesus.ece.iit.edu/~tgonnot/ECE446-F14.zip

Folder	Folder Content
Lab Manuals	ECE446 Lab Manuals (PDF 88 pages – 12 Labs)
	VHDL Combinational Circuit Tutorial
	VHDL Sequential Circuit Tutorial
	Oscilloscope User Guides
Software Manuals	ISE Design Suite, ISIM Simulator, PlanAhead User Guides
	Synthesis and Simulation Design Guide
Spartan 3E Board	Spartan 3E Board and Add-on Manuals
VHDL Modules	LCD Control Module Folder
	Clock Divider and Switch Debouncer VHDL codes
VHDL Tutorial	VHDL Cookbook

Software Downloads

Software	Download Links
Xilinx ISE Design (Download)	Xilinx ISE Design (Select WebPACK License)
Adobe Acrobat Reader (Download)	Acrobat Reader
WinRAR (Download), 7-Zip (Download)	WinRAR, 7-Zip
PDF Creator (PDF Printer Driver) (Download)	PDFCreator (1) or PDFCreator (2)