

EXPERIMENT #9

DIGITAL-TO-ANALOG (D/A) CONVERSION

1.0 Purpose

The purpose of this experiment is to introduce the student to the concepts and principles of Digital-to-Analog (D/A) conversion.

2.0 Component Requirements

<u>Quantity</u>	<u>Description (incl. Mfr.; Mfr. Part No.)</u>
1	8-bit D/A Converter; National or Motorola; DAC0808 or MC1408P8
1	Op-amp; National; LM741
Misc.	Capacitors
Misc.	Resistors

3.0 Background

The National Semiconductor DAC0808 is a eight bit monolithic digital-to-analog converter (DAC) chip. This IC will be used to study qualitatively some aspects of digital-to-analog conversion. When referring to DACs, one includes not only the actual conversion circuitry, but also any interfacing circuitry between the microprocessor system and the D/A conversion circuit, and between the conversion circuit and the output connectors. From now on, and D/A circuit using the DAC0808 to produce an analog output will be referred to as a DAC.

DACs can be used in many applications: in digital storage oscilloscopes, as computer outputs to process control systems, as the heart of an Analog-to-Digital Converter, and so on. A DAC may be characterized by any of the following parameters: the number of bits used, the output voltage/current range(s), settling time, and linearities.

DACs are available in several bit configurations: 8, 10, and 12-bit DACs are the most commonly used. Typically, an 8-bit DAC would be used for a process control application (such as controlling a valve's position), whereas the higher resolution DACs would be used for such applications as implementing an Analog-to-Digital converter for research.

The resolution of a DAC (assuming a unipolar voltage output) is its full-scale voltage divided by the number of states its holding register can have. An 8-bit DAC will thus have a resolution of $VFS/256$ volts (where VFS is its Full Scale Output Voltage).

DACs can be obtained with bipolar outputs, and these can be achieved in several different ways. One way is to take the output of the DAC and add an opposite polarity offset to it. Such an offset would usually be under computer control so that the DAC could be switched from unipolar to bipolar mode (and vice versa) at will.

Settling time is defined to be the time elapsed from the application of a full-scale step input to a circuit, to the time when the output has entered and remained within a specified error band around its final value. Settling time for a DAC is typically around 150 to 200 ns. The primary importance of settling time is in determining the upper conversion frequency for reliable operation.

Non-linearity is a problem that is very difficult to compensate for because it cannot be eliminated by user adjustment. Careful fabrication and laser trimming of internal resistor networks is used to minimize non-linearity.

4.0 Statement of Problem

In this experiment the student will use a D/A converter to generate three analog waveforms using digital means. The three waveforms will be a square wave, a sawtooth wave, and a sine wave.

5.0 Preliminary Assignment

1. Design the hardware to interface the PIA on the SANPER-1 System Board, to your external DAC. Refer to Figure 9.0 and to the SANPER-1 Memory Map.
2. Implement your hardware design on a breadboard strip.
3. Write a subroutine to initialize the SANPER-1 PIA as follows:
 - Port A lines (PA0 to PA7) are outputs
 - *IRQA interrupt disabled
4. Write a subroutine to continually accept a two digit hexadecimal value (range: \$00 to \$FF) from the terminal and output it to the DAC. Use Peripheral Data Register A of the PIA as the DAC's holding register.
5. Write a subroutine to generate a variable frequency square wave of fixed amplitude. The subroutine should alternately clear and load \$FF into the DAC's holding register, which in this case is the PIA's Peripheral Data Register A. The frequency will be determined by a "wait" loop. The delay time will be loaded in from the terminal (you may use TUTOR's Trap #14 Handler for I/O to the terminal).
6. Write a subroutine to implement a sawtooth wave generator. The input to the DAC should increment from \$00 to \$FF (one count at a time) and then immediately return back to \$00. You must incorporate a wait loop (for use in incrementing the count) whose delay time can be easily varied. Use the PIA's Peripheral Data Register A as the DAC's holding register.

7. DACs are often used for digital synthesis of other not so easily generated functions; for example, synthesis of a sine wave. If the function is periodic, the usual method is to store the sample values for the first quadrant in a look-up table, and then use this table to generate all four quadrants. Write a subroutine that uses a look-up table to generate a sine wave approximation. The entire wave is to have 128 samples, and the waveforms amplitude is to range from \$00 to \$FF. When generating the look-up table values, be sure that the error between the true sine wave and your integer sample is minimized for each point (you can do this by rounding the integer value up or down). Once again, use the PIA's Peripheral Data Register A as the DAC's holding register.

6.0 Procedure

1. Interface your breadboard strip to the SANPER-1 Educational Lab Unit. Keep the wiring as short and neat as possible.
2. Obtain an oscilloscope, and connect an oscilloscope probe to the DAC's output.
3. Execute the subroutine from Prelim #4. Enter the following values at the terminal and record the corresponding DAC output voltage: 3, 8, C, F.

Enter a value of 0, and observe the output. You may notice that a slight voltage (in the millivolt range) is present. This voltage is referred to as the "Offset Error". Make sure this error is not introduced by your oscilloscope (zero the scope). Record this offset voltage.

4. Execute the subroutine from Prelim #5. Observe and record the output waveform on the oscilloscope. Record its frequency. The op amp in your circuit is a low frequency device, and thus the settling time should be visible on the oscilloscope. Be especially careful when recording the waveform about the transition points. You may see "glitches" that occur whenever the DAC's bits do not change simultaneously. This phenomenon is analogous to the "race" condition in digital circuits.
5. Execute the subroutine from Prelim #6. Observe and record the output waveform. Record its frequency. If you see any non-linearities, make sure they are recorded in your sketch. Observe the output as the holding register changes from \$FF to \$00. At the terminal, increase and decrease the waveform's frequency. Record your results and explain your answer.
6. Execute the subroutine of Prelim #7. Observe and record the output waveform. Record its frequency. Construct a simple low pass filter (use an RC network), and filter the waveform. Carefully sketch the new waveform, and record any anomalies you may observe.

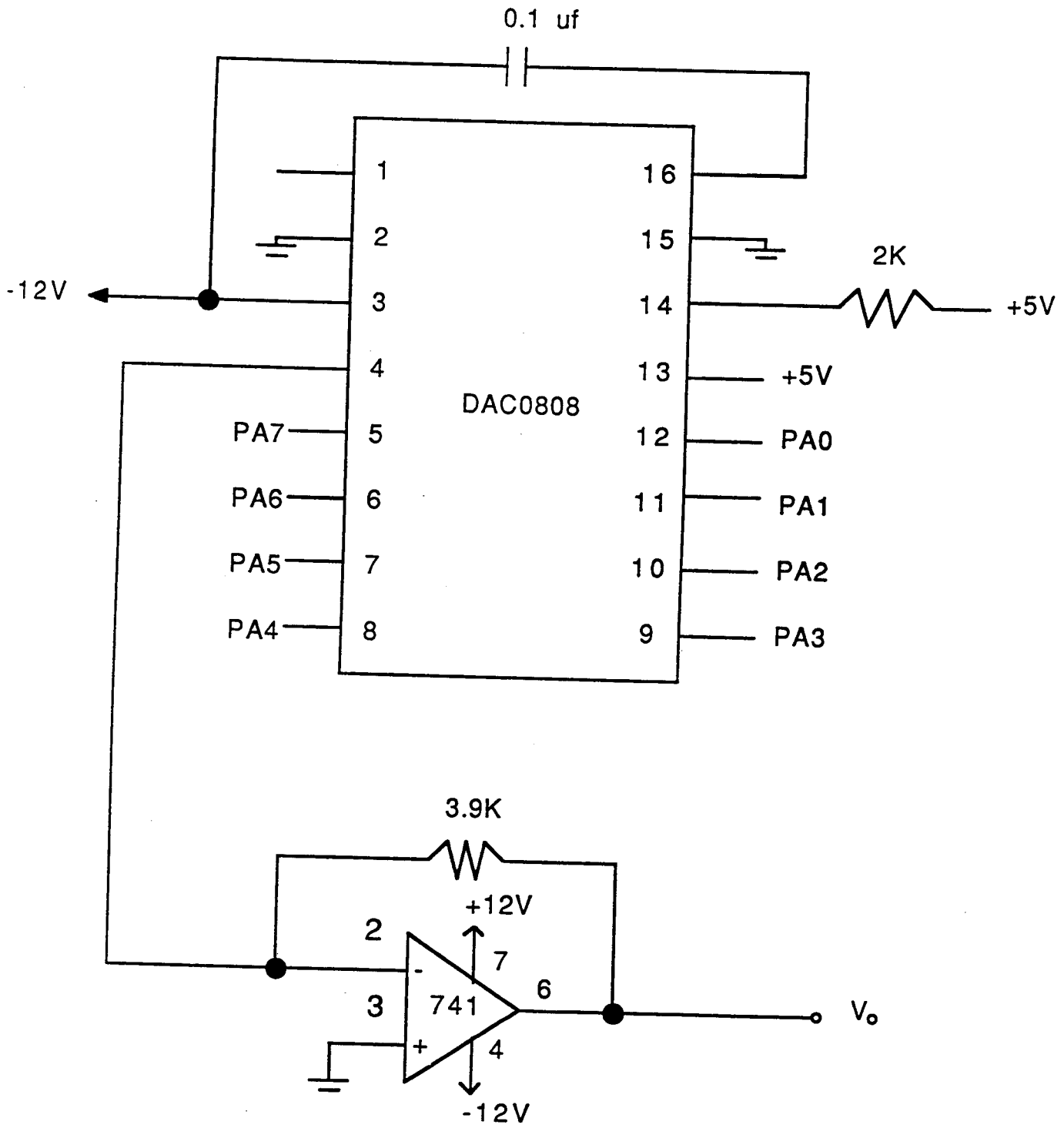
7. Demonstrate to your Lab Instructor that Procedures #4, #5, and #6 are functioning correctly.

NOTE: Keep your hardware implementation intact. You will be using this same hardware for Experiment #10.

7.0 Discussion

Submit the following to your Lab Instructor as a Final Report:

1. A schematic diagram of your hardware design.
2. Commented versions of all your subroutines.
3. The voltage readings from Procedure #3.
4. Discussion and drawings of the waveforms from Procedures #4, #5, and #6.
5. Can the DAC used in this experiment be directly interfaced to the MC68000 bus? Explain your answer.



(SAMPLE DESIGN)

FIG 9.0

DATA SHEET

MC1408-8

8-bit multiplying D/A converter

Product data
Supersedes data of 1994 Aug 31
File under Integrated Circuits, IC11 Handbook

2001 Aug 03

8-bit multiplying D/A converter

MC1408-8

DESCRIPTION

The MC1408-8 is an 8-bit monolithic digital-to-analog converter which provides high-speed performance with low cost. It is designed for use where the output current is a linear product of an 8-bit digital word and an analog reference voltage.

FEATURES

- Fast settling time: 70 ns (typ)
- Relative accuracy $\pm 0.19\%$ (max error)
- Non-inverting digital inputs are TTL and CMOS compatible
- High-speed multiplying rate 4.0 mA/ μ s (input slew)
- Output voltage swing +0.5 V to -5.0 V
- Standard supply voltages +5.0 V and -5.0 V to -15 V

APPLICATIONS

- Tracking A-to-D converters
- 2 1/2-digit panel meters and DVMs
- Waveform synthesis
- Sample-and-Hold
- Peak detector
- Programmable gain and attenuation
- CRT character generation
- Audio digitizing and decoding
- Programmable power supplies
- Analog-digital multiplication
- Digital-digital multiplication
- Analog-digital division
- Digital addition and subtraction
- Speech compression and expansion
- Stepping motor drive modems
- Servo motor and pen drivers

PIN CONFIGURATIONS

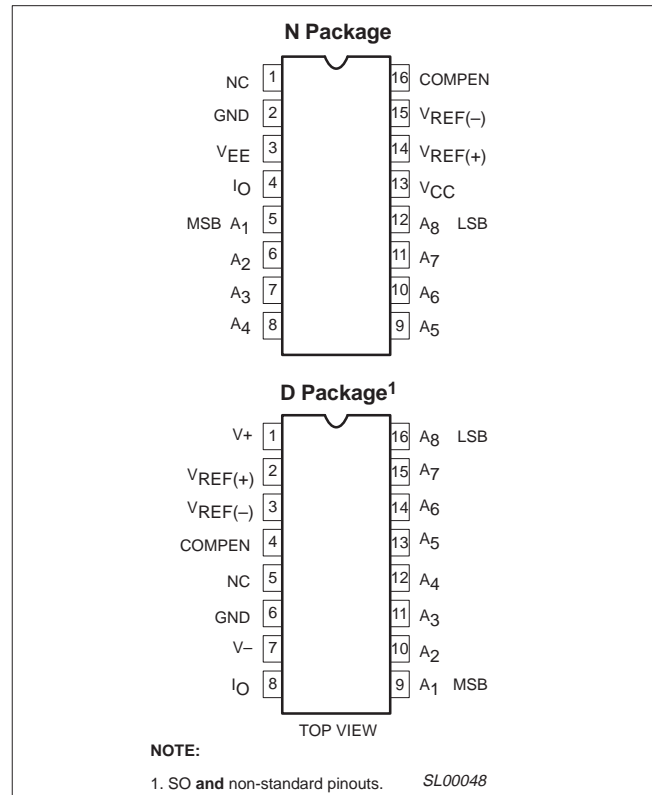


Figure 1. Pin Configurations

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C	MC1408-8N	SOT38-4
16-Pin Small Outline (SO) Package	0 °C to +70 °C	MC1408-8D	SOT109-1

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MC1408-8

BLOCK DIAGRAM

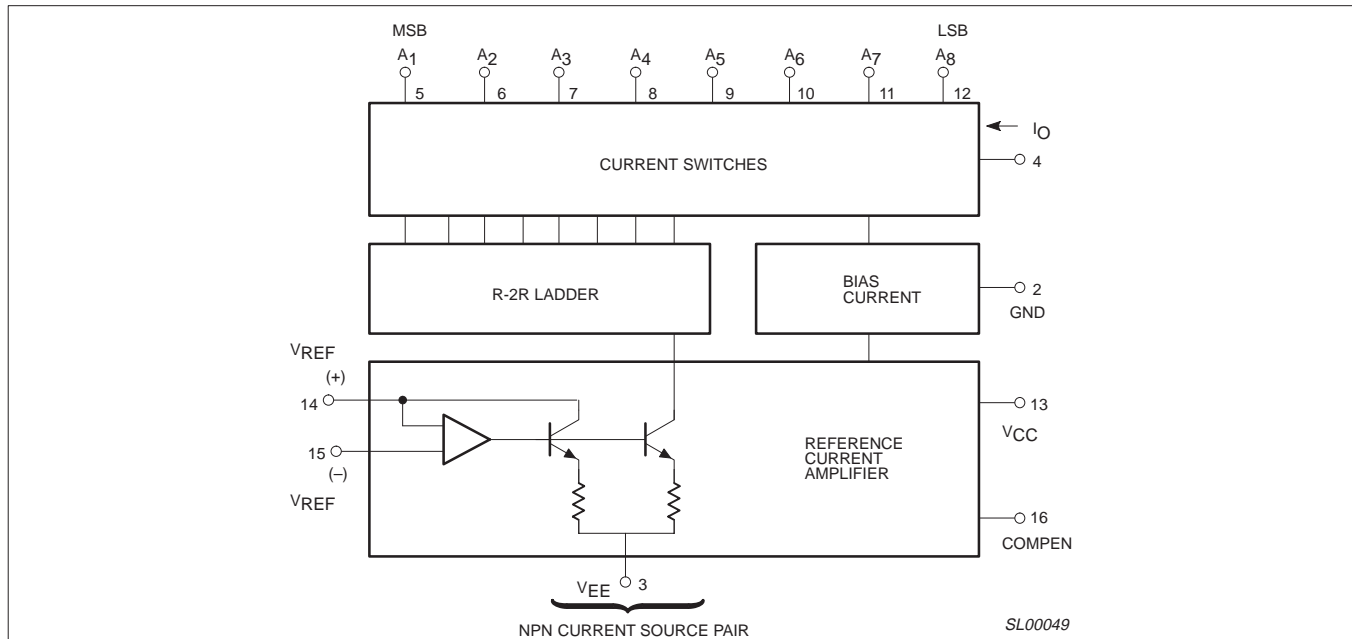


Figure 2. Block Diagram

CIRCUIT DESCRIPTION

The MC1408-8 consists of a reference current amplifier, an R-2R ladder, and 8 high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are non-inverting in operation; therefore, a high state on the input turns on the specified output current component.

The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain

feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binary-related components, which are fed to the remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Positive power supply voltage	+5.5	V
V _{EE}	Negative power supply voltage	-16.5	V
V ₅ - V ₁₂	Digital input voltage	0 to V _{CC}	V
V _O	Applied output voltage	-5.2 to +18	V
I ₁₄	Reference current	5.0	mA
V ₁₄ , V ₁₅	Reference amplifier inputs	V _{EE} to V _{CC}	
P _D	Maximum power dissipation, T _{amb} = 25 °C (still-air) ¹	1450 1080	mW mW
T _{amb}	Operating temperature range	0 to +75	°C
T _{stg}	Storage temperature range	-65 to +150	°C
T _{sld}	Lead soldering temperature (10 sec)	+230	°C

NOTES:

- Derate above 25°C, at the following rates:
N package at 11.6 mW/°C;
D package at 8.6 mW/°C

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DC ELECTRICAL CHARACTERISTICS

Pin 3 must be 3 V more negative than the potential to which R₁₅ is returned. V_{CC} = +5.0 V_{DC}, V_{EE} = -15 V_{DC}, V_{REF}/R₁₄ = 2.0 mA unless otherwise specified. T_{amb} = 0 °C to 75 °C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1408-8			UNIT
			Min	Typ	Max	
E _r	Relative accuracy	Error relative to full-scale I _O , Figure 6			±0.19	%
t _S	Settling time ¹	To within 1/2 LSB, includes t _{PLH} ; T _{amb} = +25 °C, Figure 7		70		ns
t _{PLH} t _{PHL}	Propagation delay time Low-to-High High-to-Low	T _{amb} = +25 °C, Figure 7		35	100	ns
TCl _O	Output full-scale current drift			-20		ppm/°C
V _{IH} V _{IL}	Digital input logic level (MSB) High Low	Figure 8	2.0		0.8	V _{DC}
I _{IH} I _{IL}	Digital input current (MSB) High Low	Figure 8 V _{IH} = 5.0 V V _{IL} = 0.8 V		0 -0.4	0.04 -0.8	mA
I ₁₅	Reference input bias current	Pin 15, Figure 8		-1.0	-5.0	μA
I _{OR}	Output current range	Figure 8 V _{EE} = -5.0 V V _{EE} = -7.0 V to -15 V	0 0	2.0 2.0	2.1 4.2	mA
I _O	Output current	Figure 8 V _{REF} = 2.000 V, R ₁₄ = 1000 Ω	1.9	1.99	2.1	mA
I _{O(min)}	Off-state	All bits low		0	4.0	μA
V _O	Output voltage compliance	E _r ≤ 0.19% at T _A = +25°C, Figure 8 V _{EE} = -5V V _{EE} below -10V		-0.6 +10 -5.5, +10	-0.55, +0.5 -5.0, +0.5	V _{DC}
SRI _{REF}	Reference current slew rate	Figure 9		8.0		mA/μs
PSRR(-)	Output current power supply sensitivity	I _{REF} = 1 mA		0.5	2.7	μA/V
I _{CC} I _{EE}	Power supply current Positive Negative	All bits low, Figure 8		+2.5 -6.5	+22 -13	mA
V _{CCR} V _{EEER}	Power supply voltage range Positive Negative	T _{amb} = +25 °C, Figure 8	+4.5 -4.5	+5.0 -15	+5.5 -16.5	V _{DC}
P _D	Power dissipation	All bits low, Figure 8 V _{EE} = -5.0 V _{DC} V _{EE} = -15.0 V _{DC}		34 110	170 305	mW

NOTES:

1. All bits switched.

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TYPICAL PERFORMANCE CHARACTERISTICS

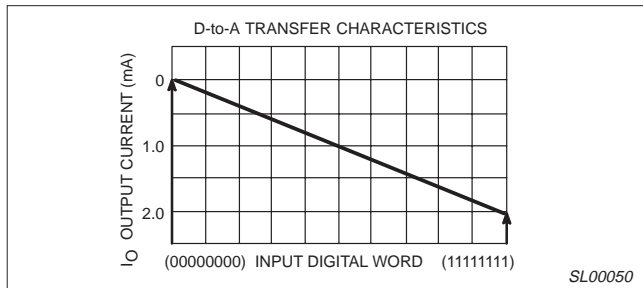


Figure 3. Typical Performance Characteristics

FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into Pin 14, regardless of the setup method or reference supply voltage polarity.

Connections for a positive reference voltage are shown in Figure 4. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. R_{15} may be eliminated and Pin 15 grounded, with only a small sacrifice in accuracy and temperature drift.

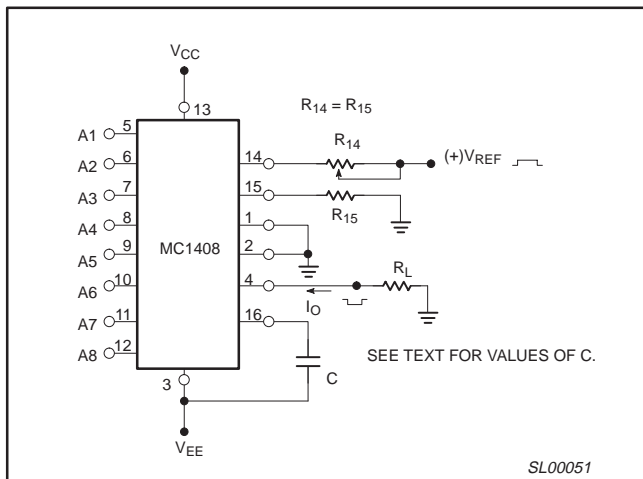


Figure 4. Positive V_{REF}

The compensation capacitor value must be increased with increasing values of R_{14} to maintain proper phase margin. For R_{14} values of 1.0, 2.5, and 5.0 k Ω , minimum capacitor values are 15, 37, and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply.)

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} , as shown in Figure 5. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3.0 V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at Pin 15.

Capacitive bypass to ground is recommended when a DC reference voltage is used. The 5.0 V logic supply is not recommended as a reference voltage, but if a well regulated 5.0 V supply which drives logic is to be used as the reference, R_{14} should be formed of two series resistors and the junction of the two resistors bypassed with 0.1 μ F to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

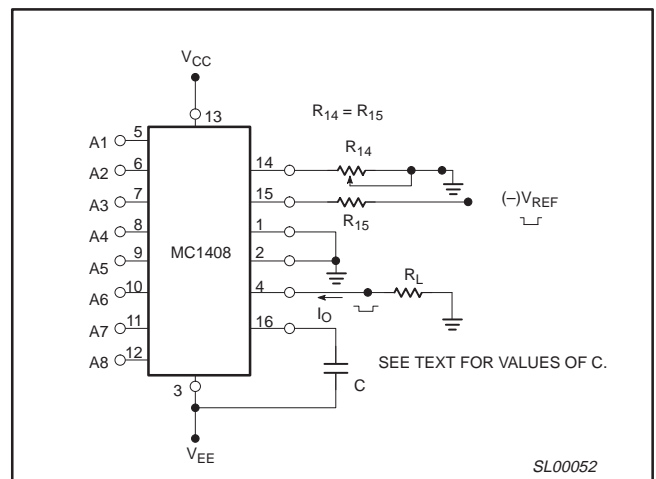


Figure 5. Negative V_{REF}

Output Voltage Range

The voltage at Pin 4 must always be at least 4.5 V more positive than the voltage of the negative supply (Pin 3) when the reference current is 2 mA or less, and at least 8 V more positive than the negative supply when the reference current is between 2 mA and 4 mA. This is necessary to avoid saturation of the output transistors, which would cause serious degradation of accuracy.

Philips Semiconductors MC1408-8 does not need a range control because the design extends the compliance range down to 4.5 V (or 8 V — see above) above the negative supply voltage without significant degradation of accuracy. Philips Semiconductors MC1408-8 can be used in sockets designed for other manufacturers' MC1408 without circuit modification.

8-bit multiplying D/A converter

MC1408-8

Output Current Range

Any time the full-scale current exceeds 2 mA, the negative supply must be at least 8 V more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full-scale accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current after zero-scale current has been nulled out. The relative accuracy of the MC1408-8 is essentially constant over the operating temperature range because of the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current; however, the MC1408-8 has a very low full-scale current drift over the operating temperature range.

The MC1408-8 series is guaranteed accurate to within $\pm 1/2$ LSB at $+25^\circ\text{C}$ at a full-scale output current of 1.99 mA. The relative accuracy test circuit is shown in Figure 6. The 12-bit converter is calibrated to a full-scale output current of 1.99219 mA; then the MC1408-8's full-scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total of $\pm 1/2$ part in 65,536, or $\pm 0.00076\%$, which is much more accurate than the $\pm 0.19\%$ specification of the MC1408-8.

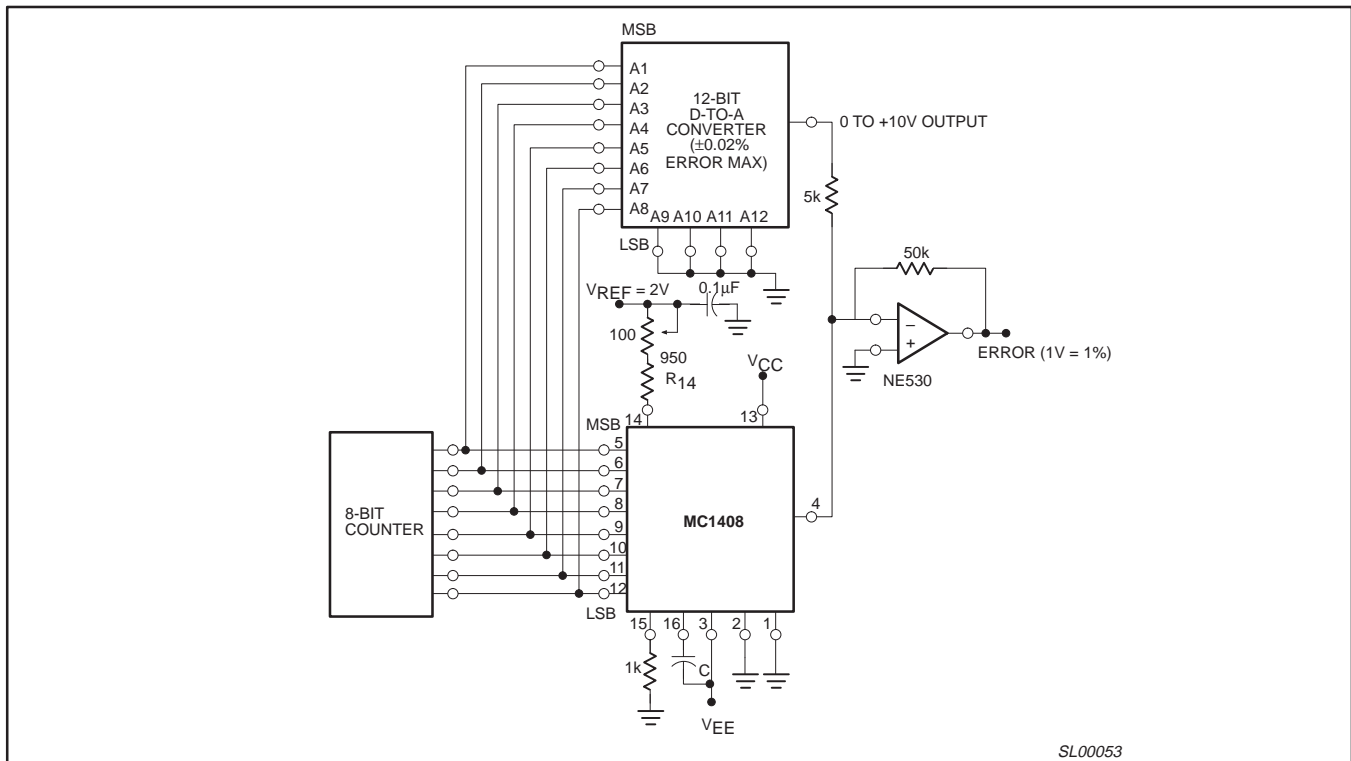
Monotonicity

A monotonic converter is one which always provides an analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The MC1408-8 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation is a DC reference current between 0.5 mA and 4.0 mA.

Settling Time

The worst case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70 ns for settling to within 1/2LSB for 8-bit accuracy. This time applies when $R_L < 500 \Omega$ and $C_O < 25 \text{ pF}$. The slowest single switch is the least significant bit, which typically turns on and settles in 65 ns. In applications where the D-to-A converter functions in a positive going ramp mode, the worst-case condition does not occur and settling times less than 70 ns may be realized.

Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, minimum scope lead length, good ground planes, and avoidance of ground loops are all mandatory.



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Figure 6. Relative Accuracy

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MC1408-8

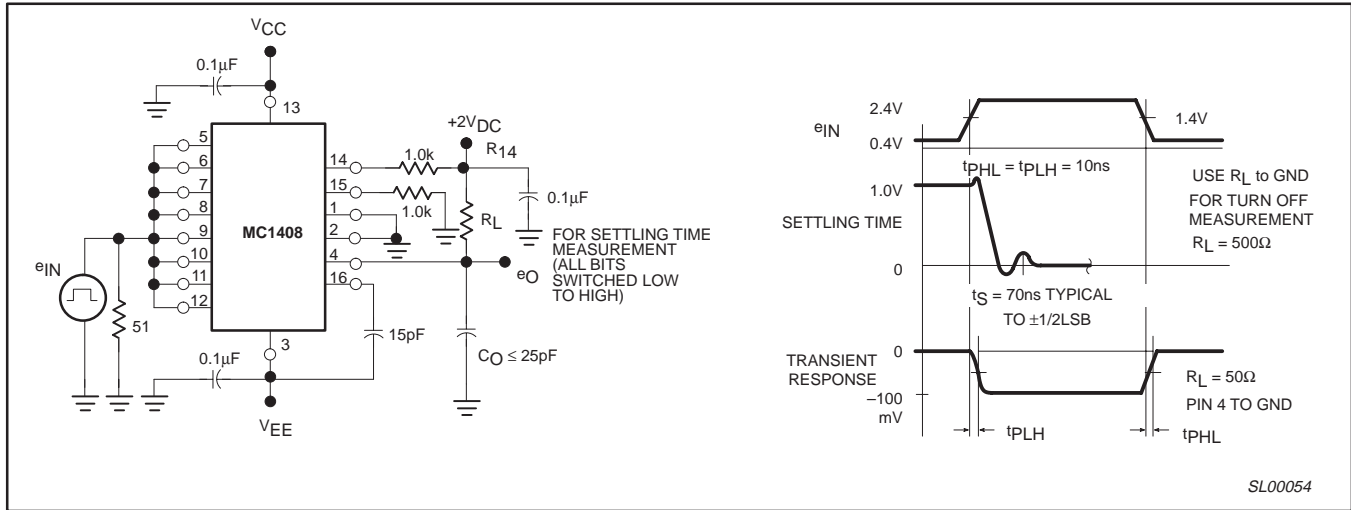


Figure 7. Transient Response and Settling Time

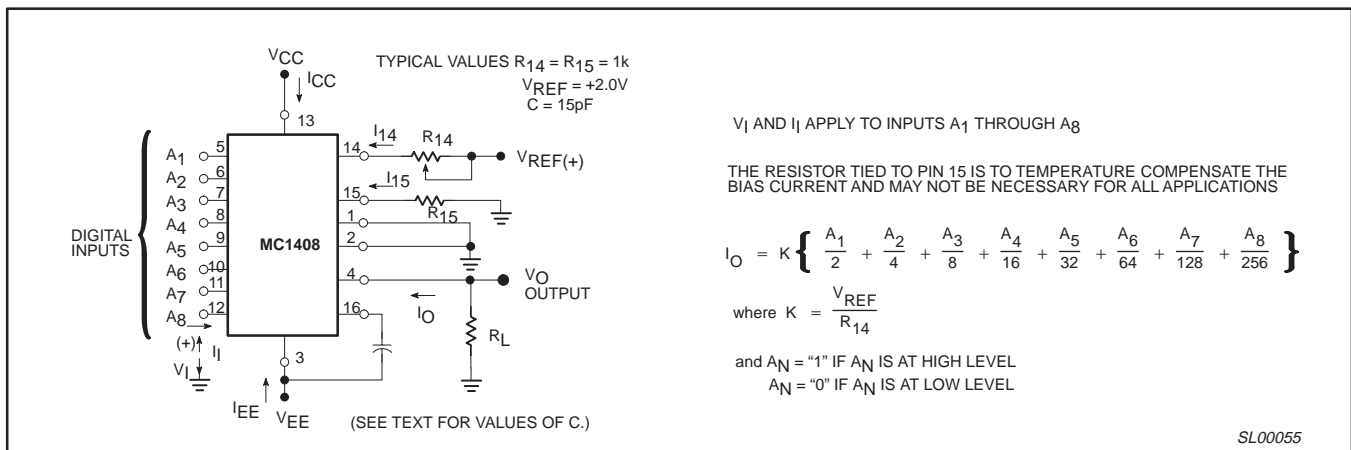


Figure 8. Notation Definitions

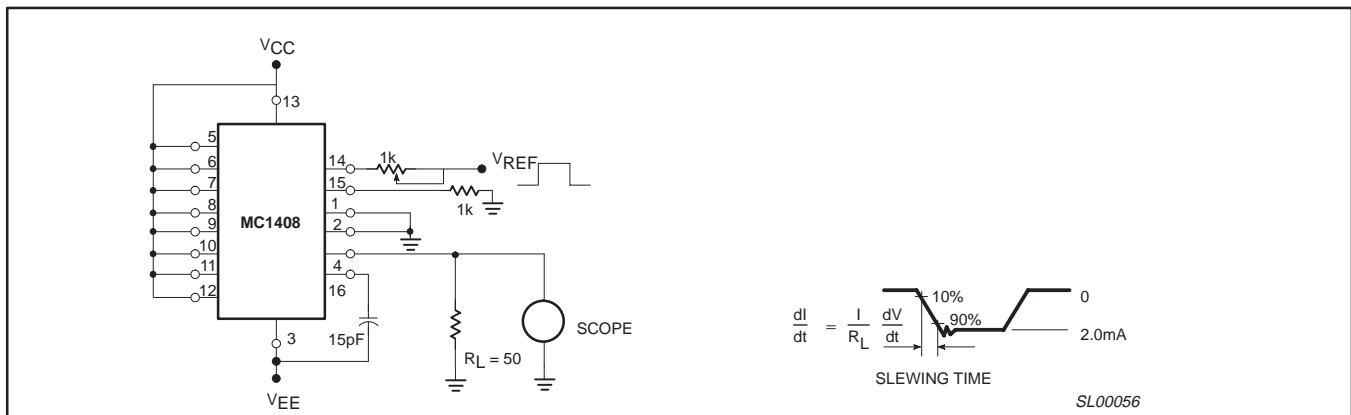


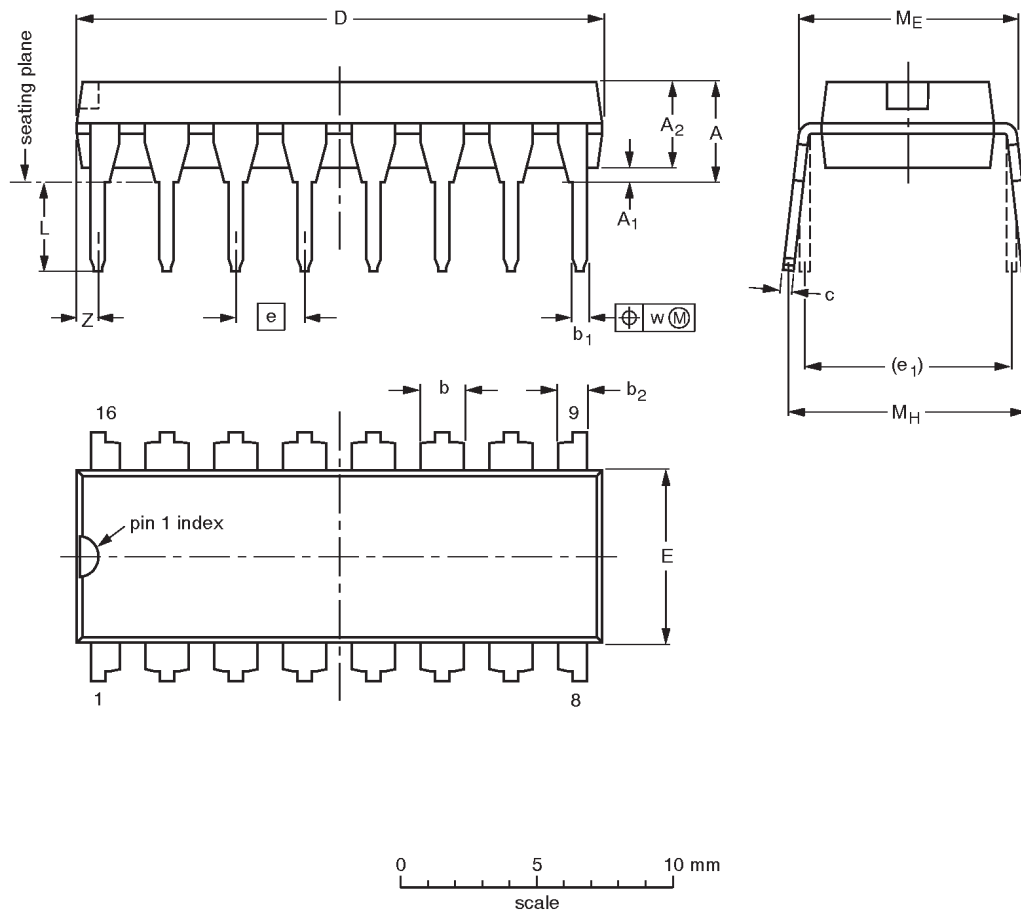
Figure 9. Reference Current Slew Rate Measurement

8-bit multiplying D/A converter

MC1408-8

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

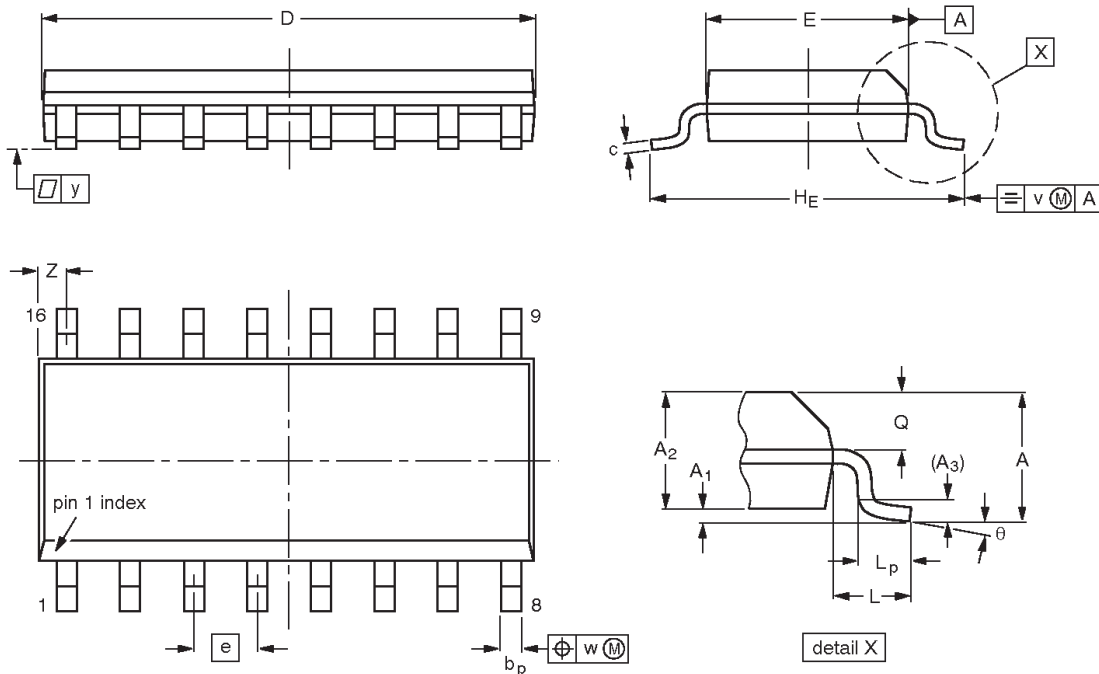
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

8-bit multiplying D/A converter

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				97-05-22- 99-12-27

8-bit multiplying D/A converter

MC1408-8

Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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