EXPERIMENT #5

MEMORY DESIGN USING STATIC RANDOM ACCESS MEMORY (RAM)

1.0 Purpose

The purpose of this experiment is to familiarize the user with the following devices and concepts:

- the MC68000's Asynchronous Bus Control Signals
- Static Random Access Memory (SRAM)
- Open Collector Devices
- the SANPER-1 ELU'S Block Select Lines

2.0 Component Requirements

Quantity:	Description: (incl. Mfr., Mfr. Part No.)
4	Static RAM, 1K x 4, Motorola, MCM2114
TBD	Misc. TTL Logic Gates (AND, OR, inverters, buffers, decoders, etc.)

3.0 Background

A. MC68000 Asynchronous Bus Interface

The MC68000 has a 16-bit data bus, and byte accesses of memory locations are permitted from either an even or an odd address. Examine the timing diagrams for both the read and write cycles.

Read Section 5, entitled "Signal and Bus Operation Description" in Motorola's MC68000 8-/16-/32-Bit Microprocessor's User's Manual (Sixth Edition). In particular, review Section 5.2.7, entitled "Asynchronous Operation".

Review the timing diagrams in Section 11 of the same manual. Specifically, examine Figure 11-4, "MC68000 Read-Cycle Timing Diagram" and Figure 11-5, "MC68000 Write-Cycle Timing Diagram". Familiarize yourself with the following 68000 control signals: *AS, *UDS, *LDS, R/*W, and *DTACK. Study the timing relationships between these signals. The time intervals are designated by a circled number, and are defined in the AC Electrical Specifications Table located immediately in front of the timing diagrams.

B. Static RAM Devices

The specifications for the MCM2114 Static RAM are included with this experiment. Examine the timing diagrams for both the read and write cycles.

C. Open Collector Devices

A standard TTL type device has two output transistors that form the output driver for the logic gate. One transistor sits about the other one. That is, the emitter of the top transistor is tied to the collector of the bottom transistor. The top transistor function acts as an active pullup for the bottom transistor. For example, a 74LS04 logic device consists of six inverters. Each inverter consists of two transistors that form the output driver. One of the transistors is used as an active pullup for the other transistor.

On the other hand, a TTL logic device with open collector outputs has only one transistor acting as the output driver. The collector of the transistor is left floating or open. Hence the name open collector output". The IC manufacturer expects the design engineer to add whatever external pullup mechanism he/she deems appropriate for the circuit to function properly.

Since a standard TTL type logic gate has a pullup mechanism built in, these outputs cannot be tied together due to possible contention problems. For example, if one of the device is trying to drive its output low, while another device is trying to drive its output high, one of the two devices will win the contention battle, while the other device will have its output transistor destroyed.

On the other hand, since devices with open collector outputs do not have a built in pullup mechanism, several open collector outputs can be tied together without damaging any of the output drivers. When all the outputs are tied together, it forms a single bus line. A resistor can then be used as an external pullup mechanism for this bus line.

A good application for devices with open collector outputs is found in microprocessor systems. If several peripheral devices exist in the system, the Interrupt Request Lines (*IRQ) or each of these devices can be connected together and then connected to the *IRQ input of the microprocessor. A resistor is connected between this *IRQ bus line and the logic supply voltage (typically +5V DC). Thus one of the peripheral devices can assert the *IRQ line without damaging the other devices. Note this technique can only be employed if the device is equipped with an open collector output on its *IRQ line.

D. The SANPER-1 ELU'S Block Select Lines

There are four Block Select lines (*Q5, *Q6, *Q7, *Q8) provided on the System Expansion Board which can be used for decoding and selecting external devices. Each of the Block Select lines was obtained by decoding address A16 through A23 and Address Strobe (*AS). Thus one of these Block Select lines can be used as an input to any additional external address decoding circuitry.

The SANPER-1 ELU Memory Map indicates the address ranges associated with each of the Block Select lines.

4.0 Statement of Problem

In this experiment the user will design and implement the hardware for a 2K x 8 bank of static random access memory. The user will write programs to test the memory to verify that each memory location can be properly read from and written to.

5.0 Preliminary Assignment

1. Design the hardware for a bank of memory that is 1K (1024 location) by 16 bits wide, residing at location $80000 to $8FFFF. Four memory integrated circuit devices will be needed. Your schematic diagram should show the address decoding circuitry, the write enable circuitry, and the static RAM devices. Each address, data and control signal to/from the CPU should be drawn separately. Do not simply draw a thick line and label it the "Address Bus" or "Data Bus". Each pin of the RAM devices should be connected to some point. Each pin of each IC should be labeled and should have a pin number associated with it.

   The RAM bank must reside somewhere within the 64K address range of $080000 to $08FFFF. However, not all of this range is available. Other hypothetical devices already occupy the following address ranges in the system.

   Device 1: $080000 - $0817FF
   Device 2: $083000 - $085FFF
   Device 3: $088000 - $088007
   Device 4: $08B000 - $08B0FF
   Device 5: $08E000 - $08E03F

   The memory bank may be placed in any non-occupied address locations within the 64K address space. The user must decode around the above existing devices so that no other device is unintentionally selected. The user must initially employ full address decoding to get within the 64K address space at $080000. The user should then determine where in the memory map to place the RAM so as to minimize the number of additional address lines required for the selecting the bank of RAM.

   HINT: Use one of the SANPER-1 ELU's Block Select Lines as part of your address decoding implementation.

   The user must also design circuitry to generate a *DTACK pulse to the MC68000 whenever this 2K byte block of memory is accessed. The user must determine if any wait states need to be inserted based upon the propagation delay through the address decoding logic and the access tomes of the RAM devices.

2. Implement your memory design on a breadboard strip.

3. Write a memory test program that operates in the following manner:

   A. Fill all of the memory to be tested with $AA.

   B. Return to the first memory location.

   C. Read the memory location. Its contents must be $AA.

   D. If the read operation is unsuccessful (contents are not equal to $AA), go to step E.

      Otherwise, write $55 into the same location. Move on to the next location. Go back to step C. When all locations have been tested, go to Step F.

   E. Since the contents are not equal to $AA, the memory test fails. Output the following information to the terminal:

      - the location at which the memory failed,
      - the value that was written, and
      - the value that was read.

      Exit the test program.

   F. Return to the first memory location.

   G. Read the memory location. It contents must be $55.

   H. If the read operation is unsuccessful (contents are not equal to $55), to Step I.

      Otherwise, write $AA into the same location. Move on to the next location. Repeat step G and H until all locations have been tested. If all tests are successful,go to Step J.

   I. Since the contents are not equal to $55, the memory test fails. Output the following information to the terminal:

      - the location at which the memory failed,
      - the value that was written, and
      - the value that was read.

      Exit the test program.

   J. If all of the memory locations can be written to and read from successfully, output a "MEMORY TEST PASSES" message to the terminal.

All memory accesses will be done on byte boundaries, allowing us to test the upper and lower data bus interfaces separately.

6.0 Procedure

1. Connect your hardware up to the SANPER-1 Educational Lab Unit.

2. Execute the memory test from Prelim #3. If your hardware passes this test, go on to Procedure Step 3. Otherwise, use the SANPER-1's hardware single step mode to troubleshoot the problem. Monitor the 68000 address, Data and Control Signal LEDs on the Front Panel of the SANPER-1 Educational Lab Unit. Compare the states of these signals to those used in your address decoding and selection logic.

3. Invoke TUTOR's Block of Memory Test (BT) command on your entire memory range, and see how well your hardware performs. If your hardware passes this test, go on to Procedure Step 4. Otherwise, divide the memory into smaller segments and repeat the test for each segment. You may want to use SANPER-1's hardware single step mode to assist you in troubleshooting the problem.

4. Demonstrate to your Lab Instructor that your hardware passes Procedure Steps 2 and 3.

7.0 Discussion

Submit the following to your Lab Instructor as a Final Report:

1. A schematic diagram of your hardware design.

2. A fully commented listing of the memory test program.

3. Discuss which address range you chose for the memory bank, and elaborate on the reasons for your selection.

4. Discuss the reasons for implementing memory tests. What conditions are you actually testing the hardware for?

5. Suggest some other bit patterns that could in used in a memory test program, and explain the reasons for your selections.

6. List the advantages and disadvantages of using Static RAMs over other types of memory devices such as EPROMS, Dynamic RAMs, etc.

MOTOROLA

MCM2114
MCM21L14

MOS
(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC
RANDOM ACCESS
MEMORY

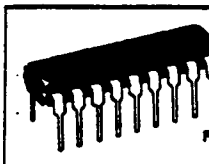
4096-BIT STATIC RANDOM ACCESS MEMORY

The MCM2114 is a 4096-bit random access memory fabricated with high density, high reliability N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of fully static operation. Data access is particularly simple, since address setup times are not required. The output data has the same polarity as the input data.

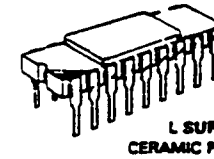
The MCM2114 is designed for memory applications where simple interfacing is the design objective. The MCM2114 is assembled in 18-pin dual-in-line packages with the industry standard pin-out. A separate chip select ($\overline{S}$) lead allows easy selection of an individual package when the three-state outputs are OR-tied.

The MCM2114 series has a maximum current of 100 mA. Low power versions (i.e., MCM21L14 series) are available with a maximum current of only 70 mA.

- 1024 Words by 4-Bit Organization
- Industry Standard 18-Pin Configuration
- Single +5 Volt Supply
- No Clock or Timing Strobe Required
- Fully Static: Cycle Time = Access Time
- Maximum Access Time
  - MCM2114-20/MCM21L14-20 200 ns
  - MCM2114-25/MCM21L14-25 250 ns
  - MCM2114-30/MCM21L14-30 300 ns
  - MCM2114-45/MCM21L14-45 450 ns
- Fully TTL Compatible
- Common Data Input and Output
- Three-State Outputs for OR-Ties
- Low Power Version Available

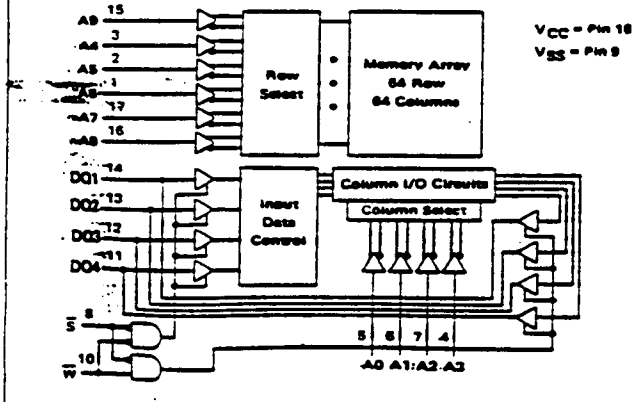


P SUFFIX
PLASTIC PACKAGE
CASE 707

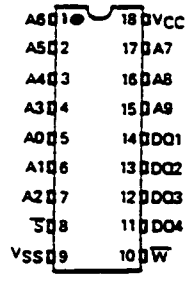


L SUFFIX
CERAMIC PACKAGE
CASE 680

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0-A9	Address Input
W	Write Enable
S	Chip Select
DQ1-DQ4	Data Input/Output
VCC	Power (+5 V)
VSS	Ground

DS9800/1-79

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	−0.5 to +7.0	V
DC Output Current	5.0	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{SS}	0	0	0	
Logic 1 Voltage, All Inputs	V_{IH}	2.0	–	6.0	V
Logic 0 Voltage, All Inputs	V_{IL}	−0.5	–	0.8	V

DC CHARACTERISTICS

Parameter	Symbol	MCM2114			MCM21L14			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{LI}	–	–	10	–	–	10	µA
I/O Leakage Current ($\overline{S}$ = 2.4 V, V_{DQ} = 0.4 V to V_{CC})	I_{LLO}	–	–	10	–	–	10	µA
Power Supply Current (V_{in} = 5.5 V, I_{DQ} = 0 mA, T_A = 25°C)	I_{CC1}	–	30	95	–	–	65	mA
Power Supply Current (V_{in} = 5.5 V, I_{DQ} = 0 mA, T_A = 0°C)	I_{CC2}	–	–	100	–	–	70	mA
Output Low Current V_{OL} = 0.4 V	I_{OL}	2.1	6.0	–	2.1	6.0	–	mA
Output High Current V_{OH} = 2.4 V	I_{OH}	–	−1.4	−1.0	–	−1.4	−1.0	mA

NOTE: Duration not to exceed 30 seconds.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Input/Output Capacitance (V_{DQ} = 0 V)	$C_{I/O}$	5.0	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

Input Pulse Levels.....0.8 Volt to 2.4 Volts
Input Rise and Fall Times.....10 ns
Input and Output Timing Levels.....1.5 Volts
Output Load.....1 TTL Gate and C_L = 100 pF

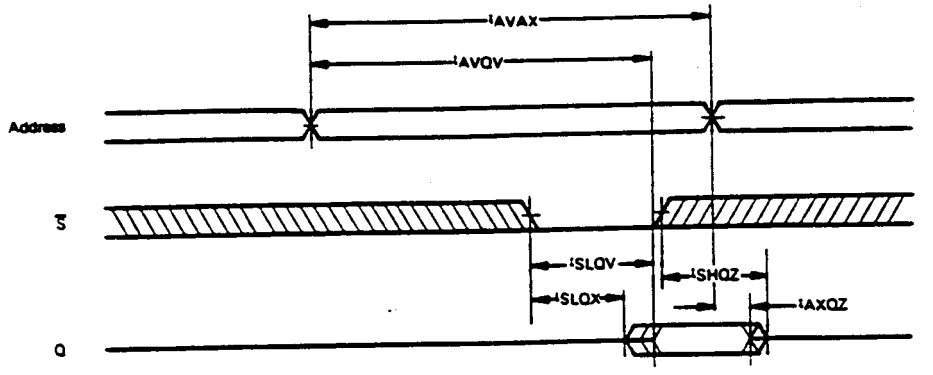
READ (NOTE 1), WRITE (NOTE 2) CYCLES

Parameter	Symbol	MCM2114-20 MCM21L14-20		MCM2114-25 MCM21L14-25		MCM2114-30 MCM21L14-30		MCM2114-45 MCM21L14-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Address Valid to Address Don't Care	t_{AVAX}	200	–	250	–	300	–	450	–	ns
Address Valid to Output Valid	t_{AVQV}	–	200	–	250	–	300	–	450	ns
Chip Select Low to Data Valid	t_{SLQV}	–	70	–	85	–	100	–	120	ns
Chip Select Low to Output Don't Care	t_{SLQX}	20	–	20	–	20	–	20	–	ns
Chip Select High to Output High Z	t_{SHQZ}	–	60	–	70	–	80	–	100	ns
Address Don't Care to Output High Z	t_{AXQZ}	50	–	50	–	50	–	50	–	ns
Write Low to Write High	t_{WLWH}	120	–	135	–	150	–	200	–	ns
Write High to Address Don't Care	t_{WHAX}	0	–	0	–	0	–	0	–	ns
Write Low to Output High Z	t_{WLQZ}	–	60	–	70	–	80	–	100	ns
Data Valid to Write High	t_{DVWH}	120	–	135	–	150	–	200	–	ns
Write High to Data Don't	t_{WHDX}	0	–	0	–	0	–	0	–	ns

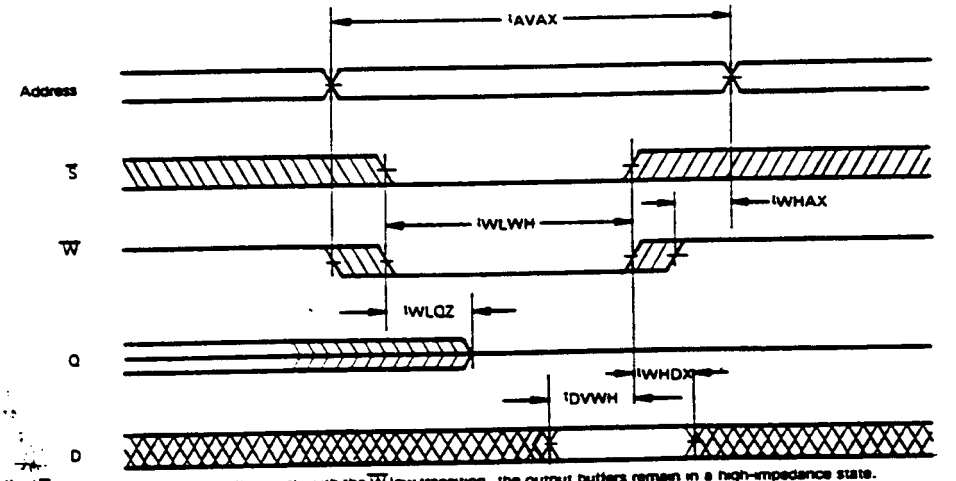
NOTES: 1. A Read occurs during the overlap of a low $\overline{S}$ and a high $\overline{W}$.
2. A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.

SRAM

READ CYCLE TIMING ($\overline{W}$ HELD HIGH)



WRITE CYCLE TIMING (NOTE 3)



3. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transition, the output buffers remain in a high-impedance state.

WAVEFORMS

Waveform Symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
	-	HIGH IMPEDANCE