CHAPTER 6

SYSTEM INPUT/OUTPUT

For system I/O, the MC68000 Educational Computer Board provides two serial communications ports, a printer compatible parallel port, an audio tape interface, and programmable timer. Chapter 6 provides a detailed discussion of each of these areas.

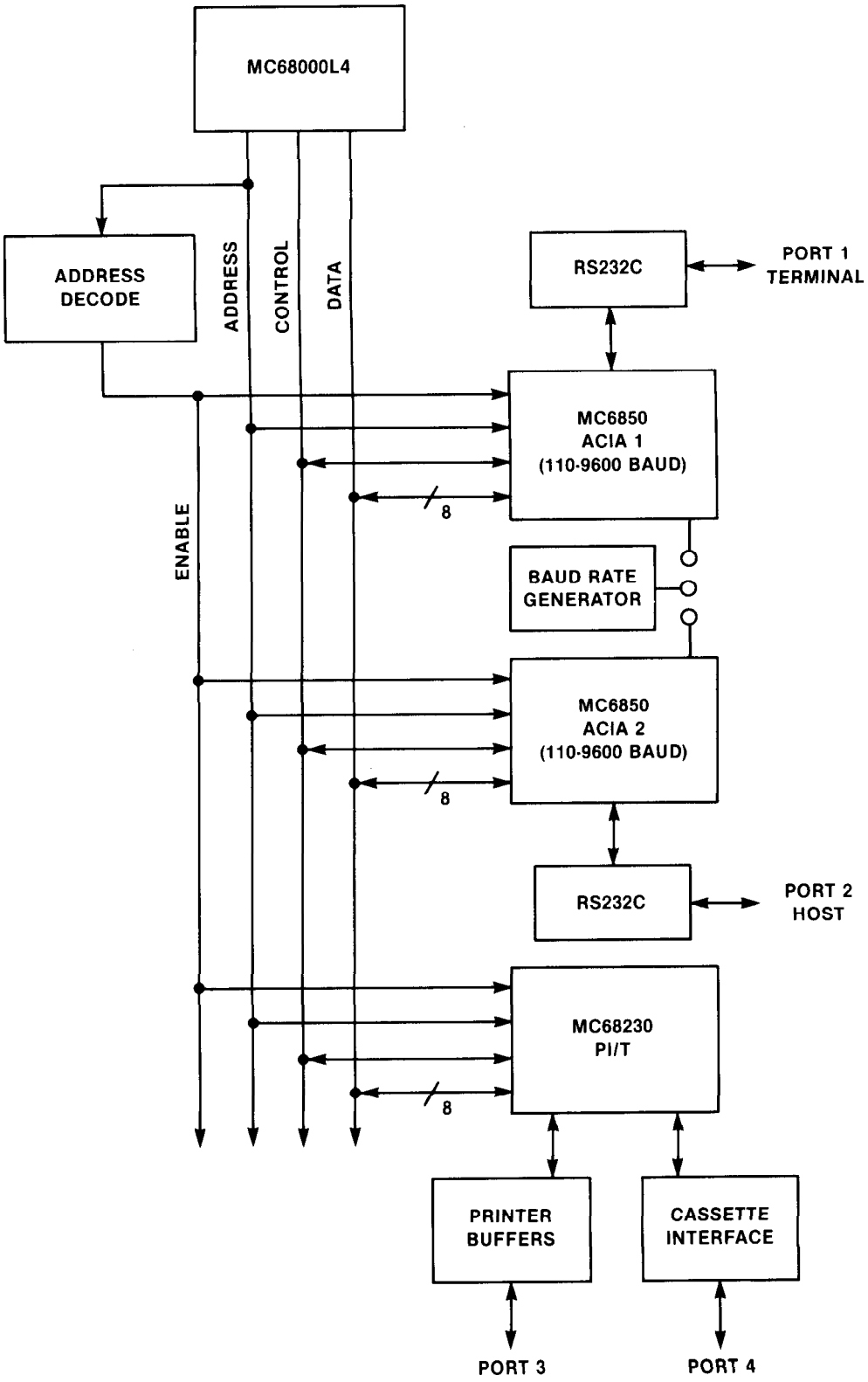

FIGURE 6-1. System I/O Block Diagram

CHAPTER 6

SYSTEM INPUT/OUTPUT

6.1 INTRODUCTION - INPUT/OUTPUT LSI DEVICES

Figure 6-1 shows the block diagram of the I/O structure for the MC68000 Educational Computer Board. Only two types of MOS LSI drives are used to interface various peripherals to the MC68000. The first device is the MC6850 Asynchronous Communications Interface Adapter (ACIA) which is a member of the M6800 family of peripheral parts. Two MC6850's are used to provide the serial communications channels of Port 1 and Port 2.

The second device type is the MC68230 Parallel Interface and Timer (PI/T) which is an M68000 family part. The Port 3 printer (parallel I/O) interface, the Port 4 cassette tape interface, and a programmable timer are all provided by this device.

6.1.1 MC6850 Asynchronous Communications Interface Adapter

The MC6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data to an M6800 synchronous parallel bus. Parallel data received from the system bus is transmitted asynchronously along with start and stop bits and parity information. Going the other way, the received serial bit stream is stripped of the start, stop, and parity bits before it is transferred to the parallel bus. Figure 6-2 shows the MC6850 block diagram. Active low signals are specified by an * following the signal name.

Information transfer and control is accomplished via four 8-bit registers within the ACIA. Two of the registers are read only registers and two are write only registers. Only one register select input is required to address all four registers; the read/write (R/W) input provides the other select control line. These registers allow programming of variable word lengths, clock division ratios, transmit control, receive control, and interrupt control.

Two bytes within the address map are needed for each of the two ACIA's present on the board. One register can be loaded and another read at each byte address. Each device has an 8-bit data interface, and the system is configured with one ACIA tied to the lower eight bits of the MC68000 data bus (D0 through D7) and the second ACIA tied to the upper eight bits (D8 through D15) of the bus. In this manner, both odd and even address locations are utilized within the address space.

As was noted, the MC6850 is a synchronous bus interface which requires that a read or write to any of its registers must by synchronized to its E clock. The E clock for the educational board is supplied by the MC68000L4 and is one-tenth (1/10) the clock frequency of the MC68000L4; that is, E is a 400 KHz clock. To interface with a synchronous device, the MC68000 can modify its normally asynchronous bus cycle to meet a synchronous cycle requirement.

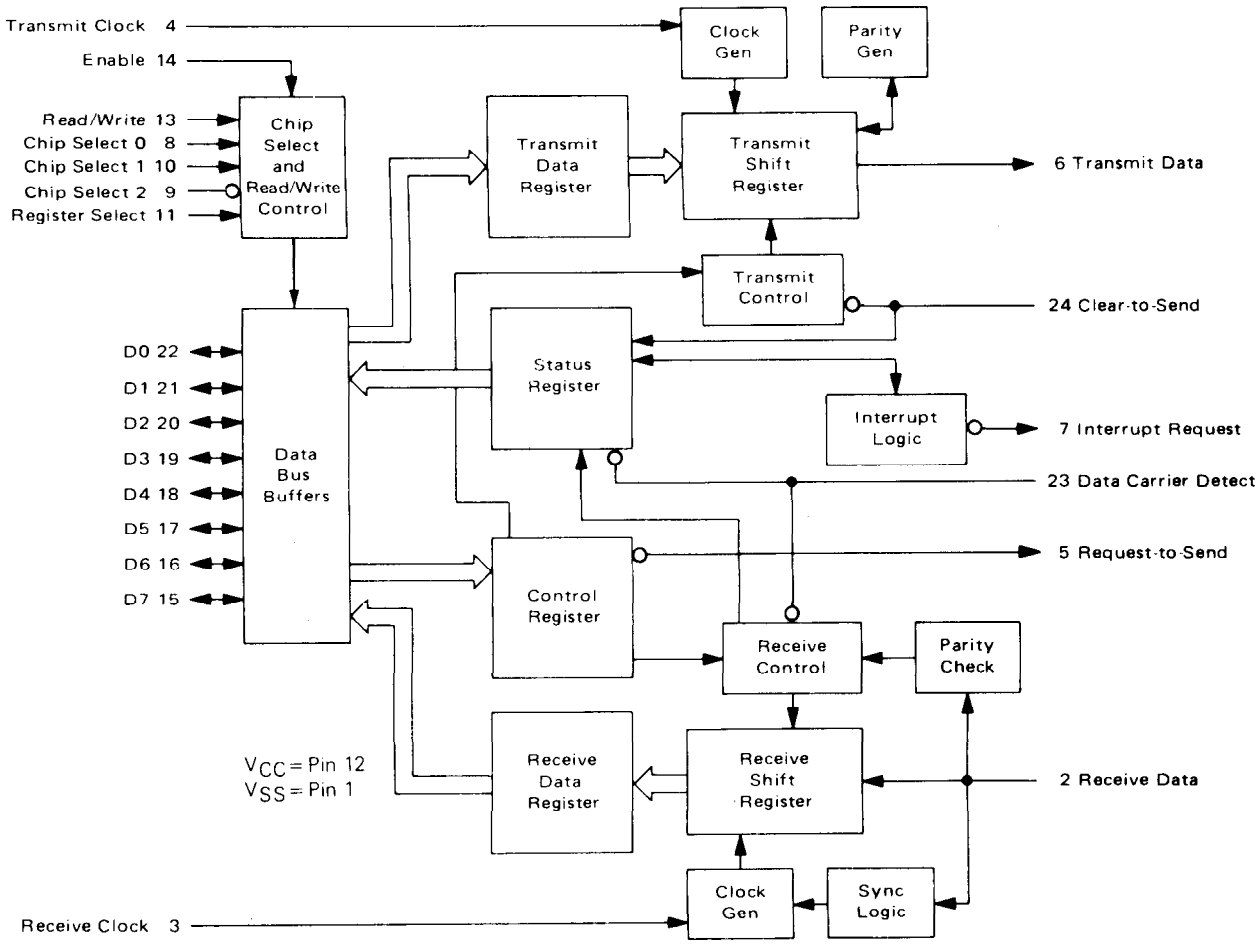

FIGURE 6-2. MC6850 ACIA Block Diagram

Hardware external to the MC68000 asserts the Valid Peripheral Address (VPA*) line whenever the MC6850's address space is accessed. The MC68000 then synchronizes itself to the E clock and asserts Valid Memory Address (VMA*). VMA* goes to the ACIA chip select logic and enables the ACIA's. When E clock is high, data is transferred. When E goes low again, the processor negates VMA* and ends the cycle.

The MC6850's are the only devices that use the MC68000's on-board synchronous interface. For more information on the MC6850, consult its data sheet.

6.1.2 MC68230 Parallel Interface and Timer

The MC68230 Parallel Interface and Timer (PI/T) provides two double buffered parallel interface ports, eight general purpose I/O pins, and a 24-bit programmable timer. The ports and the timer compose two independent sections within the PI/T. The port section consists of two 8-bit ports, Port A and Port B, four handshake lines, H1, H2, H3, and H4, and a third 8-bit port, Port C. Port C, however, is a dual function port. Six of the eight pins which make up Port C have a second function associated with the timer, interrupts, or direct memory access (DMA) requests. The MC68230 block diagram is shown in Figure 6-3.

Ports A and B can be operated individually or combined as one 16-bit wide parallel port. The parallel ports will operate in unidirectional or bidirectional modes. In the unidirectional modes, data direction registers within the PI/T determine whether the port pins are inputs or outputs. In the bidirectional modes, the data direction registers are ignored and the direction is determined dynamically by the state of the four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium, or high speed peripherals.

The other independent section within the PI/T is the timer. The timer consists of a 24-bit synchronous presettable down counter and a 5-bit prescaler. Use of the prescaler is optional. The down counter is clocked either by the output of the prescaler or by an external timer input pin (one of the Port C dual function pins). The prescaler, in turn, is clocked by either the system clock (CLK pin) or the external timer input pin. The external timer input is brought out on the J2 edge connector. The PI/T must be programmed by the user to utilize the external clock. The MC68230 timer can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. It can also be used for elapsed time measurement.

The MC68230 has 23 registers that can be addressed from the system bus. The data bus interface is eight bits wide and is tied to the lower eight bits (D0 through D7) of the system bus. Because of this, byte operations are valid only on odd addresses and accesses to upper bytes; even addresses are invalid and result in a bus trap error. The MC68230 occupies a 64-byte address space (32 words) although only 23 odd addresses are used. Note that the DTACK* will be returned anytime the other nine odd locations are accessed. These locations read as zeros, and writes to them are ignored.

The MC68230 PI/T is a complex device. This description is very short and the reader is encouraged to become more knowledgeable by referring to the MC68230 Data Sheet.

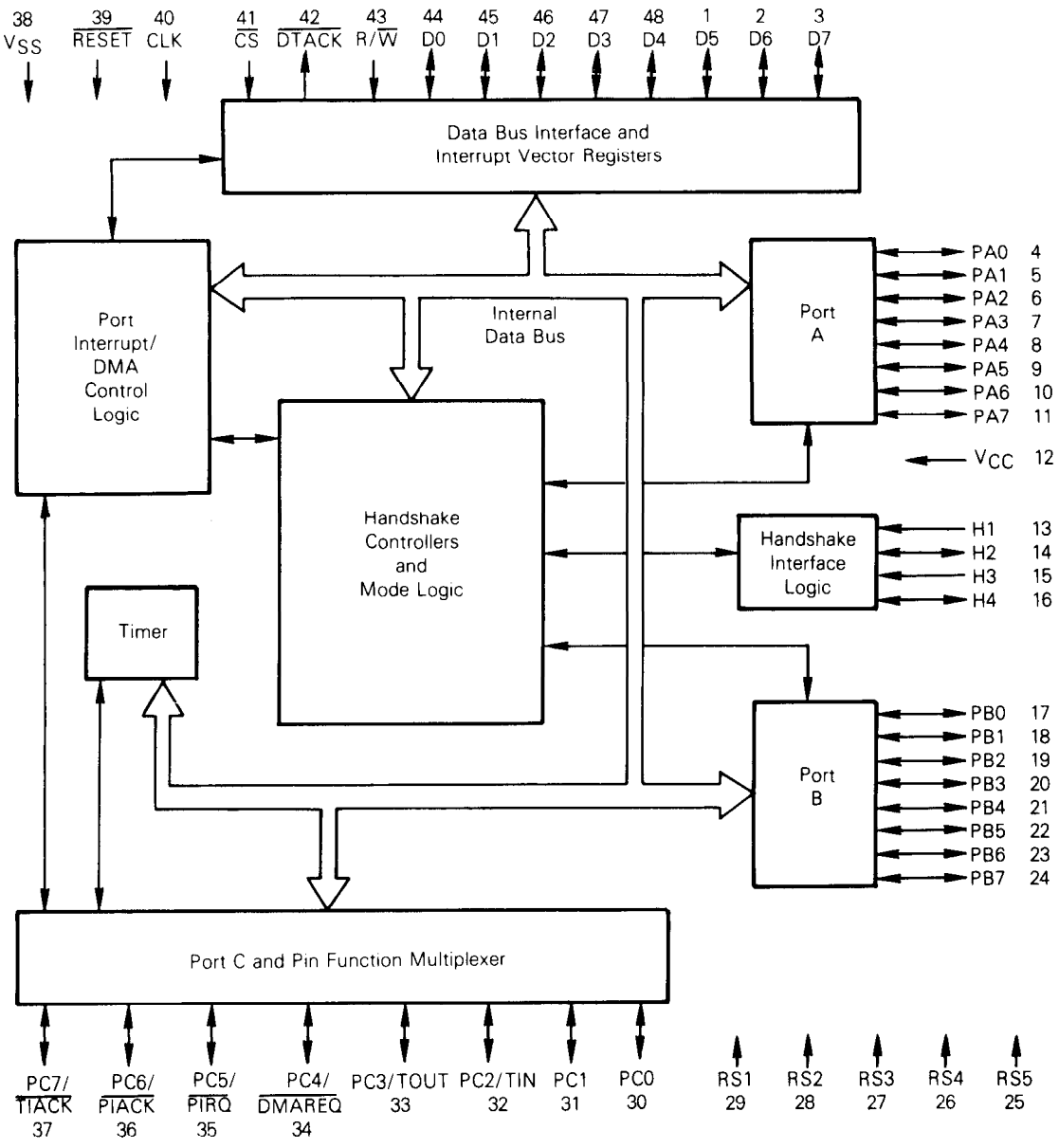

FIGURE 6-3. MC68230 PI/T Block Diagram

6.1.3 I/O Device Address Map

Page $010000-$01FFFF within the educational computer address map is reserved for the input/output devices. The registers contained within the PI/T and the ACIA's are all accessed within this page. The device addresses are not fully decoded within the page; therefore, each device can be accessed at several different areas. Refer to paragraph 7.2.2 and Table 7-1 for the address map of the entire system.

Table 6-1 shows the address map for the MC68230 PI/T, which contains 23 register locations. Within page $010000, the PI/T can be accessed any time address line A6 = 0. The MC68230 is enabled by a signal that is decoded from the upper eight address bits, A6 and LDS*. In turn, the MC68230 registers are selected via address lines A1 through A5. The PI/T responds to the following bit pattern:

```
0000 0001 XXXX XXXX X0AA AAAUDS*
                       54 321
```

The device is connected to the lower eight data lines and can be accessed only at odd byte addresses.

Table 6-2 shows the address map for the MC6850 ACIA's which each contain four registers (two are read only and two are write only). Within page $010000, the ACIA's can be accessed any time address line A6 = 1. The ACIA's are enabled by a signal that is decoded from the upper eight address bits. After being enabled, the ACIA's then use address lines A6 and A1 as well as the data strobes (LDS* and UDS*) to select registers. The ACIA's respond to the following bit pattern:

```
                                LDS*
0000 0001 XXXX XXXX X1XX XXAUDS*
                               1
```

One ACIA is accessed on the lower eight bits of the data bus, and the other is accessed on the upper eight bits of the data bus. The data strobes determine which device is selected.

TABLE 6-1. MC68230 PI/T Address Map

ADDRESS($)	PI/T REGISTER
010001	Port General Control Register (PGCR)
010003	Port Service Request Register (PSRR)
010005	Port A Data Direction Register (PADDR)
010007	Port B Data Direction Register (PBDDR)
010009	Port C Data Direction Register (PCDDR)
01000B	Port Interrupt Vector Register (PIVR)
01000D	Port A Control Register (PACR)
01000F	Port B Control Register (PBCR)
010011	Port A Data Register (PADR)
010013	Port B Data Register (PBDR)
010015	Port A Alternate Register (PAAR)
010017	Port B Alternate Register (PBAR)
010019	Port C Data Register (PCDR)
01001B	Port Status Register (PSR)
010021	Timer Control Register (TCR)
010023	Timer Interrupt Vector Register (TIVR)
010027	Counter Preload Register High (CPRH)
010029	Counter Preload Register Middle (CPRM)
01002B	Counter Preload Register Low (CPRL)
01002F	Count Register High (CNTRH)
010031	Count Register Middle (CNTRM)
010033	Count Register Low (CNTRL)
010035	Timer Status Register (TSR)

NOTE:

The PI/T address decode is redundant within page $010000. The PI/T can be accessed any time address line A6 = 0 within the page.

TABLE 6-2. MC6850 ACIA Address Map

ADDRESS ($)	ACIA REGISTER
010040	ACIA 1 - Control Register (Write Only) Status Register (Read Only)
010041	ACIA 2 - Control Register (Write Only) Status Register (Read Only)
010042	ACIA 1 - Transmit Data Register (Write Only) Receive Data Register (Read Only)
010043	ACIA 2 - Transmit Data Register (Write Only) Receive Data Register (Read Only)

NOTE:

The ACIA address decode is redundant within page $010000. The ACIA's can be accessed any time address line A6 = 1 within the page.

6.2 SERIAL COMMUNICATIONS - PORT 1 AND PORT 2

Two serial ports are provided on the MC68000 Educational Computer Board. Port 1 is normally connected to a terminal, and Port 2 provides a link to a host computer. Figure 6-4 shows a functional schematic diagram of the serial port logic. Two MC6850 ACIA's provide the interface between the computer's parallel data bus structure and the serial communications lines. Data taken from the system bus is serially transmitted and serial data received is read to the bus. The MC6850's also provide data formatting and error checking.

The serial interface is a subset of the E.I.A. RS-232C standard. Buffers provide the proper drive and levels to interface the MOS and TTL devices to RS-232C. Appendix C discusses RS-232C in more detail.

The functional mode of each ACIA is programmed via its control register (one of four on-board registers). The programmable control register sets variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. The control registers are programmed at system initialization for the selected operational modes.

6.2.1 ACIA Control Register

The ACIA control register is eight bits wide and determines the operational mode of the device. Table 6-3 lists the control bits and their corresponding states. In the normal operational mode of the educational computer, the control register is programmed with $15 which corresponds to:

- receive and transmit interrupts disabled
- 8-bit words with one stop bit, no parity
- divide-by-16 clock ratio

Some comments can be made concerning this operational mode:

a. The educational computer hardware supports ACIA interrupts (see paragraph 6.6) but the TUTOR firmware does not contain service routines for these interrupts. If the user desires to use these interrupts, he must provide the service routines.

b. The ACIA can be programmed to transmit parity bits. However, the TUTOR firmware does not check received data for parity errors. The parity error bit in the status registers is ignored.

c. Request to Send ($\overline{\text{RTS}}$) is a control line on the ACIA which allows the MPU to control a peripheral or modem by writing to the control register. $\overline{\text{RTS}}$ must be low when the educational computer is operating in its normal mode. Bringing $\overline{\text{RTS}}$ high on the Port 1 ACIA causes the board to operate in the Transparent Mode (see paragraph 6.2.6).

d. The divide-by-16 clock ratio is selected because of considerations discussed in paragraph 6.2.2.

To change the control register characters, the Port Format (PF) command (paragraph 3.5.21) can be used. The PF1 command is used to alter Port 1 (ACIA1) and the PF2 command is used to alter Port 2 (ACIA2). The user must be aware of the requirements and restrictions when altering these registers.

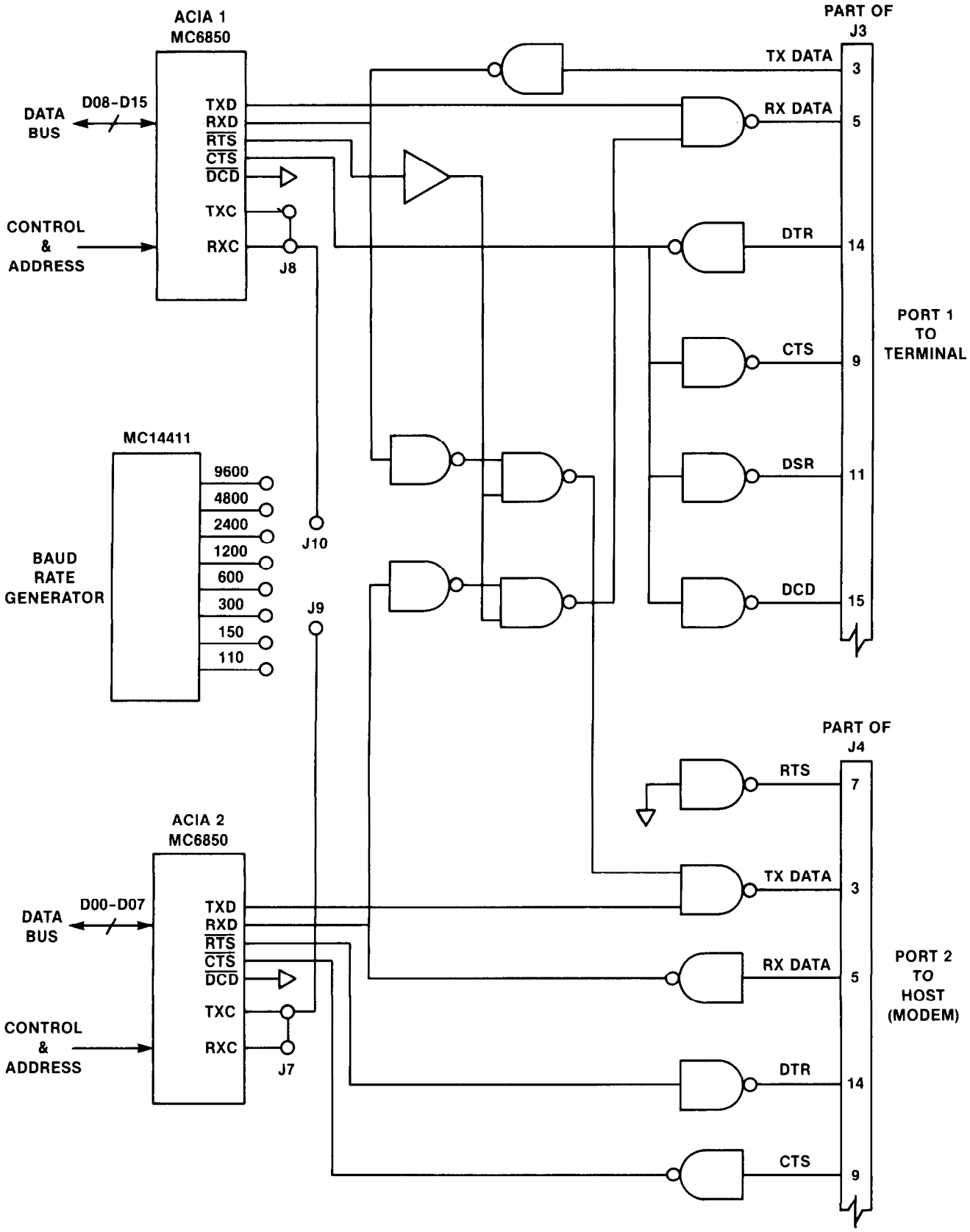

FIGURE 6-4. Serial Communications Ports Functional Schematic Diagram

TABLE 6-3. ACIA Control Register Bits

BIT 7 RECEIVE INTERRUPT ENABLE	BIT 6 & BIT 5 TRANSMIT CONTROL	BIT 4, BIT 3, & BIT 2 WORD SELECT	BIT 1 & BIT 0 COUNTER DIVIDE SELECT
0-Disabled 1-Enabled	00-$\overline{RTS}$=low Transmit Interrupt Disabled	000 - 7 bits, even parity, 2 stop bits	00 - ÷ 1 01 - ÷ 16
	01-$\overline{RTS}$=low Transmit Interrupt Enabled	001 - 7 bits, odd parity, 2 stop bits	10 - ÷ 64 11 - Master Reset
	10-$\overline{RTS}$=high Transmit Interrupt Disabled	010 - 7 bits, even parity, 1 stop bit	
	11-$\overline{RTS}$=low Transmit Interrupt Disabled Transmits a Break Level on Transmit Data Output	011 - 7 bits, odd parity, 1 stop bit	
		100 - 8 bits, no parity, 2 stop bits	
		101 - 8 bits, no parity, 1 stop bit	
		110 - 8 bits, even parity, 1 stop bit	
		111 - 8 bits, odd parity, 1 stop bit	

6.2.2 Baud Rates

The serial baud rates are jumper selectable as discussed in paragraphs 2.2.4 and 2.5.2.1. However, the clock divide ratio as selected by the control register of the ACIA affects the serial baud rate. The MC14411 Baud Rate Generator generates clocks which are actually 16 times higher in frequency than the desired serial baud rates. Under normal operation with the ACIA programmed for divide-by-16 clock ratio, the serial baud rates specified for the board result. Other non-standard clock rates could be generated.

Using a clock which is 16 times the serial bit rate allows the ACIA to synchronize the clock with the incoming serial data stream. If the ACIA clock frequency were equal to the serial bit rate, the ACIA could not synchronize the clock and the data.

6.2.3 TUTOR Firmware I/O Drivers

As previously stated, the ACIA's are programmed at system initialization. The I/O firmware drivers can then be used to control communication using the serial ports. The drivers for the terminal and host ports are very similar. Characters to be transmitted are converted to ASCII-coded bytes and are placed in a RAM buffer. Pointers to the beginning and end of the buffer are saved. The buffer is transmitted one byte at a time by writing each byte into the appropriate ACIA Transmit Data Register. The ACIA inserts the previously selected start, stop, and parity bits and performs the parallel to serial conversion.

The Transmit Data Register is double-buffered; that is, it can accept a second byte to be transmitted while it is actually transmitting a first byte. Bit 1 of the ACIA Status Register (TDRE) is polled by the processor to determine when the data has been transferred from the Transmit Data Register so that new data may be entered while the old data is being transmitted serially. An interrupt can also be generated if the transmitting interrupt is enabled.

The maximum rate at which the processor can enter data is a function of the serial baud rate and the number of bits transmitted for each byte (including start, stop, and parity bits):

$$\text{Update rate (bytes/second)} = \frac{\text{baud rate (bits/second)}}{\text{number of bits/byte (bits/byte)}}$$

As an example, for 9600 baud and eight data bits with one stop bit and one start bit, the maximum update rate is 960 bytes/second or approximately one byte every millisecond.

The input driver routines monitor bit 0 (RDRF) of the ACIA Status Register to determine when a new byte of data has been received. As above, this bit is polled by the processor; however, an interrupt can be generated. The ACIA removes the parity, start, and stop bits, sets the appropriated status bits, and performs the serial-to-parallel conversion. The received data is typically encoded ASCII, and a carriage return signifies the end of the input string. As the incoming data is received, the processor stores it in a buffer. After the carriage return is received, processing begins on the data stored in the buffer.

6.2.4 Port 1 Terminal Interface

ACIA1 (U13) is used as the terminal interface and is connected to the upper half (D08-D15) of the system bus. As previously described in Table 6-2, its registers reside at even addresses $010040 and $010042 within the memory map.

The RS-232C interface of Port 1 (J3) appears as a modem to the terminal connector. Referring again to Figure 6-4, six signal lines are supported through RS-232C buffers. The ACIA interfaces to three of these including transmit data (TX DATA), receive data (RX DATA), and data terminal ready (DTR). Some terminals require other lines to be present including clear to send (CTS), data set ready (DSR), and data carrier detect (DCD). These signals are driven back to the terminal; however, they are merely a connection to DTR which shows that the terminal is attached and ready.

As part of the power-up and reset firmware routines, the ACIA is reset by setting control register bits 0 and 1. This ensures that the device is master reset before selecting the operating configuration. This bus-programmed master reset also releases the internal reset that occurs at power-on. The programmed reset must be applied prior to operating the ACIA.

To initialize the ACIA, a $15 is written to the control register. Information can now be sent or received. As previously described, the driver routines interface with the device to transmit and receive data.

One special feature of Port 1 is that the processor also monitors the framing error status bit (FE) of ACIA1. Detection of this error form shows activation of the BREAK key, which causes the processor to abort the present activity and return to TUTOR.

6.2.5 Port 2 Host Interface

ACIA2 (U12) forms the host interface and is connected to the lower half (D00-D07) of the system bus. Its registers reside at odd addresses $010041 and $010043 within the memory map.

The RS-232C interface of Port 2 (J4) appears as a "terminal" to the host or modem connector. Five signal lines are supported including TX DATA, RX DATA, RTS, DTR, and CTS.

ACIA2 is reset and initialized similar to ACIA1. Operation for transmitting and receiving data occurs in a similar manner.

While transmitting or receiving data via Port 2, TUTOR also monitors Port 1 for the BREAK key. This allows the user to abort a function which uses Port 2 communications.

6.2.6 Transparent Mode

As described in paragraph 3.5.23, the Transparent Mode (TM) command within TUTOR connects serial Ports 1 and 2 together. In this manner, the user terminal appears connected directly to the host computer, bypassing the MEX68KECB.

To enter this mode, the Request To Send ($\overline{RTS}$) pin of the ACIA1 is brought high by writing a 10 into bits 6 and 5 of the control register. The RTS line gates the transmit and receive data paths so that the serial ports are tied together; that is, the incoming data line of Port 1 is gated through to the outgoing line of Port 2, and the incoming data line of Port 2 is gated through to the outgoing data line of Port 1. ACIA1 continues to receive incoming data from Port 1.

In the transparent mode, the educational board is not directly involved in data transmission between the terminal and the host. The ECB monitors the data transmission from the terminal and restores normal operation upon detecting a predetermined exit character. The character is selected with the TM command.

6.3 PARALLEL I/O PORT3 - PRINTER INTERFACE

Port 3 of the MC68000 Educational Computer is a parallel I/O interface and is configured to support a Centronics type printer. The MC68230 PI/T is used to provide the register and bus interface required for this I/O. The MC68230 supports a wide range of operating modes through programming of its 23 internal registers, however, this discussion focuses on this particular application. Refer to the MC68230 Data Sheet for a description of other modes.

6.3.1 Signal Line Configuration

Figure 6-5 shows the MC68230 and the buffer devices used on Port 3. The parallel interface consists of 8 data lines buffered as outputs (PA0 through PA7) which are associated with handshake lines H1 and H2, and eight unbuffered data lines (PB0 through PB7) which can be used as bidirectional lines and are associated with handshake lines H3 and H4.

The signal line designations used for connector J1 are those corresponding to the Centronics interface. The 8 buffered output data lines are PD0 through PD7. Handshake line H2 is also buffered as an output strobe and is called DATA STROBE*. Handshake line H1 is an unbuffered input strobe and is designated ACKNOWLEDGE*.

Only three of the unbuffered data lines (PB0 through PB2) are used in the printer interface. Signals from the printer indicate:

a. SELECT - when the printer is selected.

b. PAPER OUT - when the printer is out of paper.

c. BUSY - when the printer is busy.

Any of these conditions is valid when the signal is high. The printer is unable to receive information when PAPER OUT or BUSY is activated and when SELECT is not activated.

The additional handshake lines H3 and H4 are also used. H3 is the FAULT* input from the printer which indicates a printer fault condition such as out of paper or deselect. This input is not monitored by the TUTOR firmware because the individual conditions are used as shown above. Finally, output handshake line H4 is buffered and drives signal INPUT PRIME*. When INPUT PRIME* is driven low, the input buffer within the printer is cleared and the printer logic is initialized.

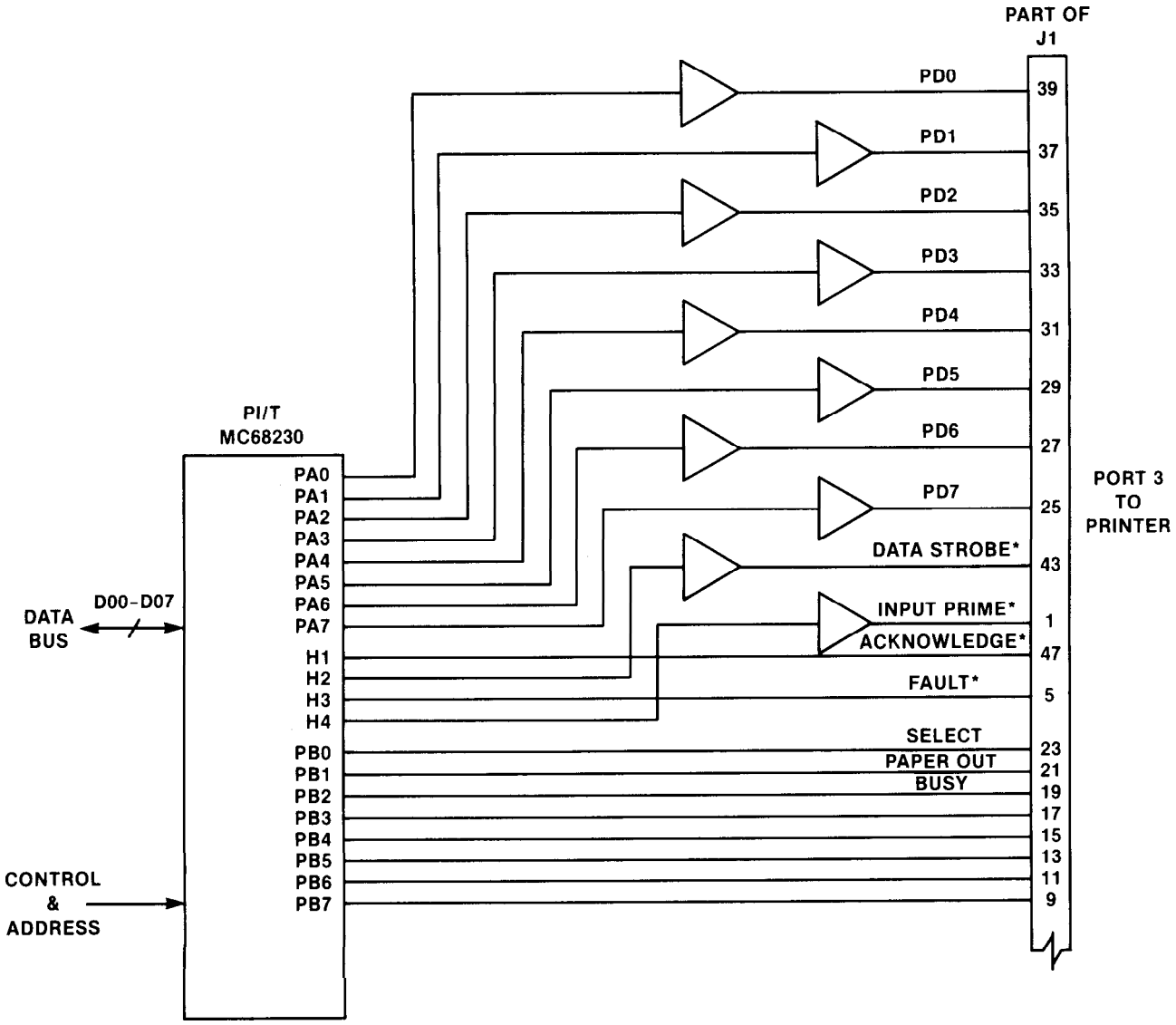

FIGURE 6-5. Printer Interface Port 3 Functional Schematic Diagram

6.3.2 Programming the PI/T

As part of the power-up and reset routines the PI/T registers are initialized, modes are selected, and the direction of data at the various ports is defined. The necessary PI/T registers are shown in Table 6-4. The base address of the MC68230 is $10001. The registers are addressed on the lower half of the MC68000 data bus; i.e., odd address locations. Bits in the Port General Control Register (PGCR) are programmed to select the unidirectional 8-bit mode with all handshake lines active low. The port mode control field of the PGCR should be altered only when H12 enable and H34 enable fields are zero. For this reason, these two fields are initially set to zero when the port mode control field is first programmed. They are later set to one to enable the handshake lines.

The Port Service Request Register is cleared; direct memory access and interrupts are not used. Port A bits are designated as all outputs and Port B as inputs by programming the associated data direction register. A one in any bit indicates an output; zeros indicate inputs. Submodes are determined by the bits of the appropriate port control register. Bit 3 of each of the two port control registers can be a one or a zero depending upon the required state of the H2/H4 handshake lines. Initially, these bits are cleared. The data registers are used to send characters to the printer and to check the status lines. Handshake status bits are displayed in the port status register.

The last step of the initialization sequence is to reset and initialize the printer by pulsing INPUT PRIME* (handshake line H4) low. This is done by setting and then clearing bit 3 of the Port B control register. At this point, the printer is initialized but not selected. It must be selected by the user using the select button; a select code is not sent by the MEX68KECB to automatically select the printer.

Characters can now be sent to the printer. All 7-bit ASCII encoded characters from $20 through $7F, $0D (carriage return), and $0A (line feed) are acceptable. Other codes below $20 are not printable and will be replaced by $2E (period). All 8-bit codes will be masked to 7 bits.

When a printable character has been obtained, it is written to the Port A data register and the printer is strobed to indicate valid data. The status bits PB0-PB2 are then checked. If an error exists the message PRINTER NOT READY will be sent to Port 1. The status lines are monitored until the error condition is removed or the break key is entered at the terminal. After the error is removed, the same byte is sent again. Before the next byte can be sent the PI/T must receive an acknowledge from the printer indicating that it has accepted the data. Bit 0 of the port status register indicates whether either of the Port A output latches can accept new data (ACKNOWLEDGE* received) or whether both latches are full.

TABLE 6-4. PI/T Registers Used in Printer Interface

Register Address	Register Bit 7	6	5	4	3	2	1	0	Register Name	Programmed Value
$10001	Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense	Port General Control Register	00ØØ 0000
$10003	*	SVCRQ Select		Interrupt PFS		Port Interrupt Priority Control			Port Service Request Register	0000 0000
$10005	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port A Data Direction Register	1111 1111
$10007	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port B Data Direction Register	0000 0000
$1000D	Port A Submode		H2 Control			H2 Int Enable	H1 SVCRQ Enable	H1 Stat Ctrl	Port A Control Register	0110 Ø000
$1000F	Port B Submode		H4 Control			H4 Int Enable	H3 SVCRQ Enable	H3 Stat Ctrl	Port B Control Register	1010 Ø000
$10011	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port A Data Register	————
$10013	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port B Data Register	————
$1001B	H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S	Port Status Register	————

NOTE: A Ø (zero with a slash) in the programmed value indicates that the bit is programmed with different values depending on operation.

6.4 AUDIO TAPE INTERFACE - PORT 4

The audio tape interface is implemented using the 16-bit timer on the MC68230 and two I/O lines. Information is sent to the tape as a serial bit stream. A digital one is represented by one period of a 50% duty cycle 2000-Hz square wave, whereas, a 1000-Hz 50% duty cycle square wave represents a logic zero. The serial data rate is then somewhere between 1000 and 2000 baud, depending on the bit stream being sent.

Saving and loading programs on tape is discussed in paragraphs 4.5.1 and 4.5.2. In this discussion, the circuitry and operation of the tape interface are discussed in detail.

6.4.1 Data Transfer Baud Rate

As with any data transfer using ASCII encoding, the effective baud rate measured by the time required to transfer a block of data is lower than the data rate on the transmission line. ASCII encoding generates a two-digit byte for every hex digit of data (for example, a 4 becomes ASCII $34). This reduces the transfer rate by one-half. In addition, S-records require overhead bytes such as type of S-record, address of data, number of bytes in the record, and checksums to be sent along with the data. This results in additional baud rate reduction of approximately one-third. The effective baud rate of the tape interface is between 300 and 500 baud, as opposed to the serial transmission rate of 1000 to 2000 baud.

6.4.2 Circuit Operation

The interface circuitry between the MC68230 and the tape player/recorder is shown in Figure 6-6. Port C of the PI/T provides two I/O lines for the tape interface.

Data is sent out via output PC1 of the PI/T. This output drives a voltage divider formed by R1 and R2 and is then AC-coupled to pin 3 of connector J2 designated DATA OUT. The voltage level from the PI/T is reduced by approximately 10 to 1 to avoid overdriving the tape recorder input.

The auxiliary input of the tape recorder is generally used, however, the microphone input will also work with most recorders. In either case, several adjustments should be made prior to recording. If there is no automatic record level control, use the volume control to adjust the record level (about mid-range). If a tone control is present, it should be set to get the best high frequency response. This corresponds to a "tinny" sound for audio recordings. Also, a clean or erased tape provides best results.

Information comes back from the tape player via pin 1 of connector J2 designated DATA IN. This signal passes through the interface circuit shown in Figure 6-6. Comparator U4B is used to square up the slowly changing transitions coming from the tape and produce rapid transitions. Diodes CR1 and CR2 limit the input voltage swing of the comparator. Approximately 450 millivolts of hysteresis is used on the comparator.

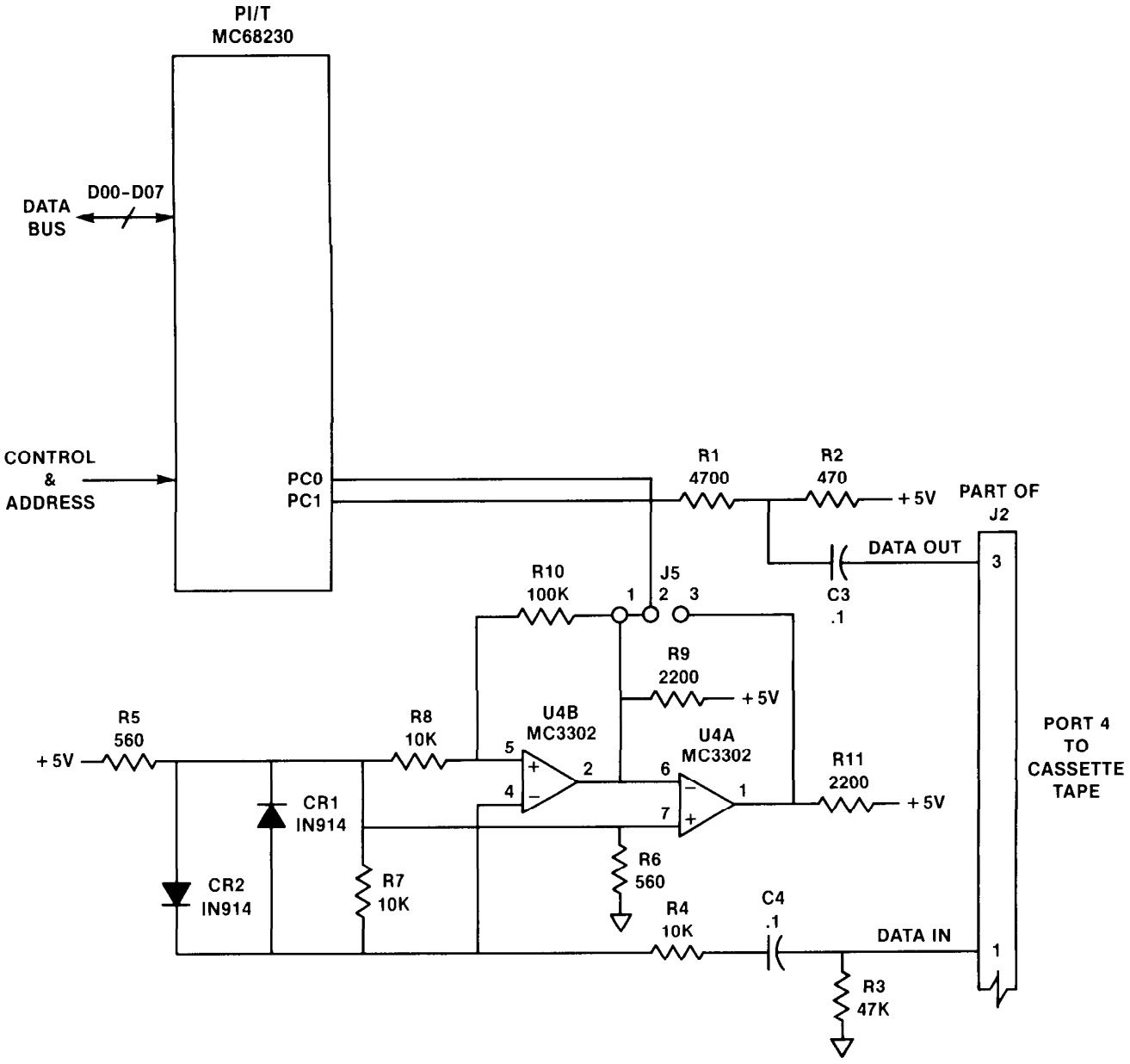

FIGURE 6-6. Audio Tape Interface

The second comparator, U4A, is used to invert the output of U4B. This may or may not be required, depending on the type of tape recorder used. Some tape recorders play back a signal which is inverted from the original input signal; others return a noninverted signal. Comparator U4B inverts the playback signal; if the tape player does not produce a second inversion, one must be produced on the educational computer board using U4A in order to provide the proper signal to the tape driver/receiver firmware. The firmware expects a noninverted signal. Jumper J5 can be used to select the second inversion. See the following paragraph 6.4.3.

6.4.3 Selecting Noninverted Data

Figure 6-7 shows the location of header J5 which is used to provide noninverted data to the tape receiver firmware (refer to Figure 6-6). If it is determined that the tape player does not invert the data, the user must change the polarity of the signal provided to the MC68230. Perform the following steps to invert the data:

a. Cut the signal trace between pin 1 and pin 2 of header J5 on the back side of the printed circuit board. BE CAREFUL -- be sure to cut the correct trace; it is approximately 1/8 inch long.

b. Place a plastic cap jumper on header J5 between Pin 2 and Pin 3.

If it is ever desired to restore the signal to the original configuration, the plastic cap jumper can be placed between pin 1 and pin 2.

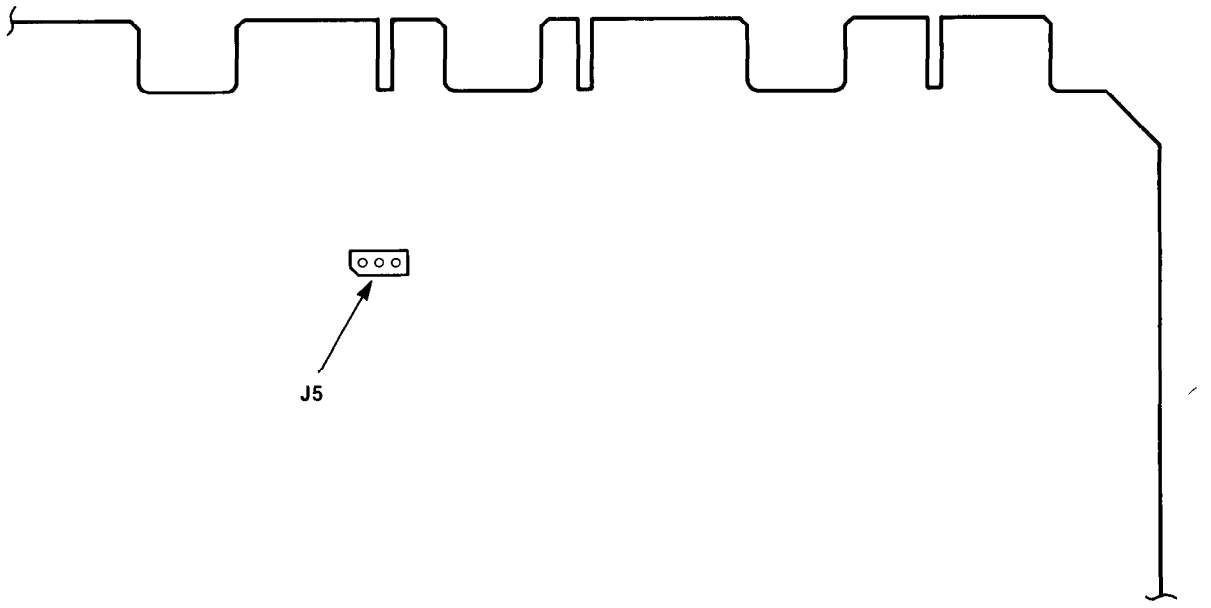

FIGURE 6-7. Header J5 Location

6.4.4 Programming the PI/T

Port C of the PI/T and the on-board timer are used by the tape driver/receiver firmware to send and receive tape data. Bit 1 of Port C (PC1) is specified as an output to transmit data via the data direction register (all other Port C bits are inputs). The 24-bit timer is used to generate and measure the time intervals for the 2000 Hz and 1000 Hz square waves. The timer prescaler is used and is clocked by the falling edge of the 4-MHz system clock.

To transmit data, the following sequence of events occurs. After obtaining the bit that will be sent, the driver firmware loads a count representing one half the required period (i.e., 500 microseconds for 1 kHz and 250 microseconds for 2 kHz) into the counter preload registers. Port C bit 1 is set high and the timer is started. Bit 0 of the timer status register is monitored until the specified time has elapsed, causing this bit to be set. At this point the timer is stopped, PC1 is cleared, and the timer is restarted. The counter is automatically loaded with the contents of the preload registers. The status register is again monitored to determine the end of the specified time period and the completion of the output sequence. Another bit is obtained and the output sequence is repeated.

To receive data, the tape input firmware measures the time between rising edges of the input square wave to determine whether a logic one or zero is being sent. It can now be seen why the polarity of the incoming signal is so important. If the signal is inverted then the elapsed time measured is really the time between the middle of one square wave (falling edge) and the middle of the next square wave of the original wave form. The data would obviously become garbled and lost.

The first step in the input sequence is to initialize the Port C data direction register and then look for a low-to-high transition at PC0. This synchronizes the firmware to the incoming signal and no data is lost because at least one null character (eight zeros) is always recorded before any data.

When the high level is received at PC0, the timer is started using the same mode as the output routine. However, the preload value is different. PC0 is monitored until a low level followed by a high level is received, at which point the timer is stopped and the value in the count register is read and saved. The timer is restarted. The period of the square wave is determined from the difference between the original timer preload value and the count left in the timer when it is halted. Additional bits are received in the same way.

6.5 PI/T TIMER

The MC68230 PI/T contains a 24-bit synchronous down counter that can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. Also, it can be used for elapsed time measurement.

The PI/T timer is loaded from three 8-bit Counter Preload Registers. The 24-bit counter can be clocked from the output of a 5-bit (divide-by-32) prescaler, or directly from a clock source. The clock source can be the 4 MHz system clock (tied to the CLK input) or an external clock tied to the TIN pin. Several different modes can be programmed by the user.

The counter signals occurrence of an event primarily through zero detection (when the counter value is zero). The zero detect status (ZDS) bit is set in the Timer Status Register (TSR). This is the only bit in the TSR. Also, an interrupt can be generated with the zero detect.

The timer is fully configured and controlled by programming the 8-bit Timer Control Register. It controls (1) the choice between the Port C operation and the timer operation of three timer pins, (2) whether the counter is loaded from the Counter Preload Register or rolls over when zero detect is reached, (3) the clock input, (4) whether the prescaler is used, and (5) whether the timer is enabled.

The contents of the counter can be read via the three count registers. The counter must be stopped to get an accurate reading when accessing these registers.

To summarize, the PI/T timer is fully controllable and available to the user. For detailed information on using the timer, the MC68230 Data Sheet should be referenced. On the Educational Computer Board, the following applies:

a. The timer can be clocked from the 4 MHz system clock or an external clock.

b. The external clock can be connected to pin 5 of connector J2. The maximum allowable clock frequency with an external signal is 4 MHz when using the prescaler and 125 KHz when not using the prescaler.

c. The timer registers are all available from the bus (addresses $010021 through $010035). See Table 6-1.

d. The timer can generate a level 2 interrupt on the MC68000. See paragraph 6.6 for details.

6.6 SYSTEM INTERRUPTS

The I/O devices discussed in this chapter have the ability to generate interrupts when they require attention. Also, the ABORT function is activated via the interrupt structure. Interrupts can be generated on the Educational Computer Board from the following sources:

a. The ABORT switch generates the equivalent of an unmaskable interrupt when activated.

b, Serial Ports - For each MC6850 ACIA, an interrupt can be generated when either the Transmit Data Register is empty requiring another byte of data or the Receive Data Register is full containing a new byte of information. In either case, the interrupt condition will not cause an interrupt unless enabled in the ACIA status register. An enabled interrupt condition pulls the $\overline{IRQ}$ pin of the ACIA low.

c. Parallel Port 3 - The parallel port of the MC68230 has an independent interrupt capability. The dual function pin $\overline{PIRQ}$ provides an active low parallel port interrupt request when enabled.

The $\overline{\text{PIRQ}}$ output is activated when any of the status bits associated with handshake lines H1, H2, H3, and H4 goes to a 1. Bits 3, 4, 5, and 6 of the PI/T Port Service Request Register (PSRR) enable and disable the $\overline{\text{PIRQ}}$ and $\overline{\text{PIACK}}$ functions and define whether interrupt or DMA requests are generated from activity on the H1 and H3 handshake lines. Each of the four individual interrupt conditions can be selectively enabled in the Port A and Port B control registers.

d. PI/T Timer - The MC68230 timer can also independently generate an interrupt. TOUT provides an active low timer interrupt request when enabled. The timer generates an interrupt when the 24-bit counter decrements from $000001 to $000000. Bits 7, 6, and 5 of the timer control register (TCR) are used to enable the timer interrupt function and control timer operation.

e. M6800 IRQ - A special auto-vectored interrupt request level is provided for the wirewrap area.

6.6.1 MC68000 Interrupt Structure

The MC68000 recognizes seven interrupt priority levels. The interrupt priority levels are numbered from one to seven with level seven having the highest priority (the equivalent of a non-maskable interrupt). The MC68000 status register contains a three-bit mask which indicates the current processor priority level. Interrupts are inhibited for priority levels less than or equal to the current processor priority. An interrupt request is made to the processor by encoding the interrupt request level on the interrupt request lines with a zero indicating no interrupt requests.

The interrupt priority levels assigned on the MC68000 Educational Computer are shown in Table 6-5. The ABORT button is assigned the level 7, non-maskable interrupt. Level 4 is reserved for an M6800 type bus interface interrupt that can be implemented in the wirewrap area of the board. Level 1 is not assigned.

All interrupts except those generated by the MC68230 are serviced through autovectoring. Autovectoring is used when the interrupting device cannot provide the processor with an exception vector from which the processor can fetch the address of the interrupt service routine. During the processor interrupt acknowledge cycle, VPA* must be asserted to indicate that an internally generated vector is to be used. The processor then generates a vector number which is determined by the interrupt level number. The seven autovector numbers are vector numbers 25 through 31 (decimal). During an interrupt acknowledge cycle for interrupt levels 7, 6, 5, and 4, VPA* is asserted by the ECB hardware and the autovector is used. During an acknowledge cycle for level 3 or 2 interrupts, the interrupting device (MC68230) must provide an 8-bit vector number to the processor.

TABLE 6-5. Interrupt Priority Levels

INTERRUPT LEVEL	INTERRUPTING DEVICE	AUTOVECTOR NUMBER (DECIMAL)
7	ABORT Button*	31
6	ACIA2 (Host)*	30
5	ACIA1 (Terminal)*	29
4	M6800 IRQ*	28
3	PI/T Parallel Ports ($\overline{\text{PIRQ}}$)	Not Used
2	PI/T Timer (TOUT)	Not Used
1	Not Used	Not Used

*Autovectored Interrupts

The 8-bit interrupt vectors associated with $\overline{\text{PIRQ}}$ and TOUT are written into the Port Interrupt Vector Register (PIVR) and the Timer Interrupt Vector Register (TIVR), respectively. Only the upper six bits of the port interrupt vector number are programmed by the user. Each of the four interrupt sources has its own vector which together appear as a contiguous block of four vector numbers whose common upper six bits are programmed in the PIVR. The lower two bits are determined by the interrupt source:

H1 Source - 00
H2 Source - 01
H3 Source - 10
H4 Source - 11

If a vector number is not programmed in the appropriate interrupt vector register before an interrupt occurs, the MC68230 will supply 15 (decimal) for the vector number, where 15 is defined as the uninitialized interrupt vector in the MC68000 exception vector table.

When acknowledging MC68000 compatible vectored interrupts, MC68230 input pins $\overline{\text{PIACK}}$ and $\overline{\text{TIACK}}$ are used. When $\overline{\text{PIACK}}$ or $\overline{\text{TIACK}}$ is asserted and a port or timer interrupt request is being asserted, the PI/T places the corresponding vector on the data bus. The appropriate pin is asserted by the system logic during an interrupt acknowledge cycle. $\overline{\text{PIACK}}$ and $\overline{\text{TIACK}}$ are dual function pins; the appropriate function is selected in the Port Service Request Register or in the Timer Control Register.

6.6.2 Interrupt Software Routines

The TUTOR firmware does not support any interrupts except level 7 which is the ABORT function. Although the ECB hardware can generate interrupts for levels 2 through 6, it is the user's responsibility to provide the interrupt service routines and to initialize the MC68000 exception vector table with the starting addresses of the service routines.

The MC68000 translates an 8-bit vector number into an address as shown in Figure 6-8. The vector number is multiplied by four (shifted left two places) to generate an address within the exception vector table. At this location in RAM, the starting address (32 bits) of the interrupt handler routine is stored. All 8-bit vector numbers -- both autovectored and user supplied -- are treated in the same way.

A23	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
All Zeros		v7	v6	v5	v4	v3	v2	v1	v0	0	0

FIGURE 6-8. Address Translated from 8-Bit Vector Number

To use the interrupts, the user must enable the interrupts through the appropriate peripheral control registers, program the vector numbers where required on the MC68230, initialize the exception vector table, and, finally, supply the interrupt handler routines. All of these tasks must be part of the user program and its system initialization procedures.