Logic Analyzer Familiarization

Objective

In this lab assignment you will become familiar with the HP 54620A Logic Analyzer and its use as a debugging tool. Using your SRAM circuit, you will learn how to setup the logic analyzer to trigger on different conditions and display multiple logic signals.

Background

You have already become familiar with the use of an oscilloscope for displaying voltage versus time. The oscilloscope can be used as a tool for logic circuits as wells as analog circuits since different voltage ranges represent different logic values. The biggest drawback of doing this is that oscilloscopes have a limited number of channels. In complex logic circuits we may want to observe several signals simultaneously.

Logic analyzers alleviate this problem. They display logic values that represent the value of digital signals versus time. Logic analyzers can display several of these signals simultaneously, making them ideal for debugging complex circuits. Logic analyzers are no substitute for an oscilloscope when debugging tricky analog problems because they can display only logic one and zero values. However, they excel when you are attempting to debug complex sequential circuits.

Logic analyzers operate by repeatedly sampling data inputs and temporarily storing them while searching for trigger condition. If no trigger condition is detected, stored values are overwritten by new values as they are sampled. If the trigger condition is detected, then the stored data is shown on the display so that the user can see the values of the signals before, during, and after the trigger condition. In the logic analyzer, these values are displayed as traces similar to an oscilloscope's traces. The traces can be formatted to display binary, octal, hexadecimal or user-defined values.

A major advantage of logic analyzers is that they can collect this data at high speed, making it possible to test circuits at full clock speed where errors are likely to occur. Logic analyzers are extremely useful when debugging sequential circuits, which may contain many signals that change at different times. Examining the signals with a logic analyzer allows you to see if the circuit is behaving properly and, if not, to isolate the source of the problem. Unlike an oscilloscope, which triggers only on a single signal, logic analyzers can trigger on patterns of multiple inputs, making it possible to specify exactly the sequence of events that you wish to examine. Figure 1 shows a diagram of the HP 54620A logic analyzer's front panel. Notice the similarity between its controls and controls on in an oscilloscope. This similarity is intentional to make the logic analyzer easy to learn and use.

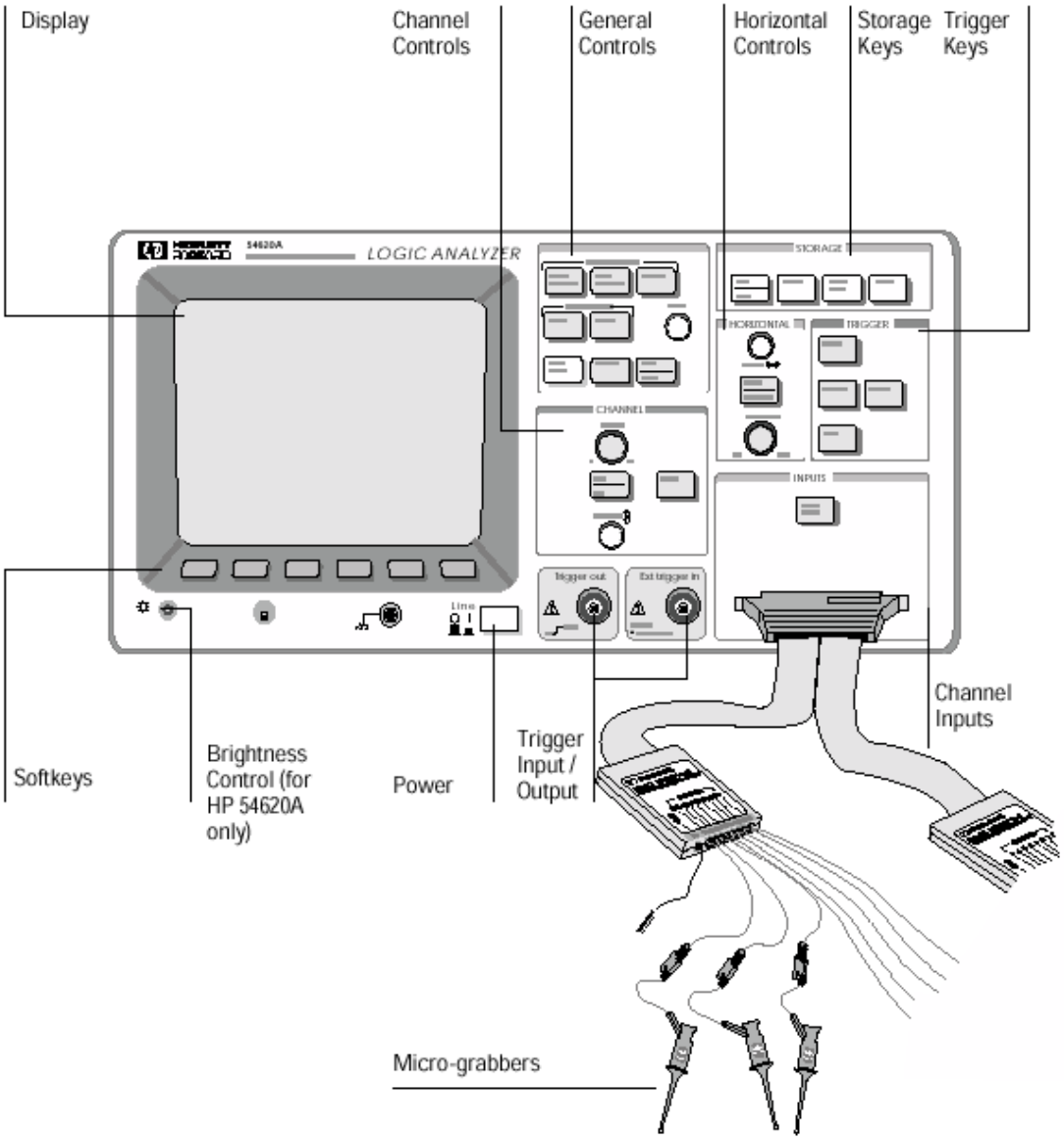

Figure 1 - HP56420A Front Panel & Probes

Logic Analyzer Basics

There are 16 channel probes connected to the front of the logic analyzer via a ribbon cable. The probes are grouped together into two pods of eight probes and each probe has a unique number between 0 and 15 that corresponds to its channel number. There's also a ground probe connected to each pod that should be attached to the circuit's ground.

Each probe is connected to a micrograbber. The micrograbber is used to attach to wires or integrated circuit pins. Please be gentle using the probes and micrograbbers - **they are easy to break**. Always use micrograbbers - **do not insert wires directly into the probes since this may damage the springs inside them**.

To connect a probe to test your circuit, first turn off the power then connect the micrograbber to the circuit in one of the following ways: 1) to the end of a short piece of wire. Plug one end into the breadboard at your test point and attach the micrograbber to the other end or 2) connect the micrograbber directly to an integrated circuit pin. Be careful to avoid shorting two pins together though. It is important to turn off the power so you do not short out your circuit when making the connections. Figure 2 shows an example of connecting the micrograbbers to a circuit under test.

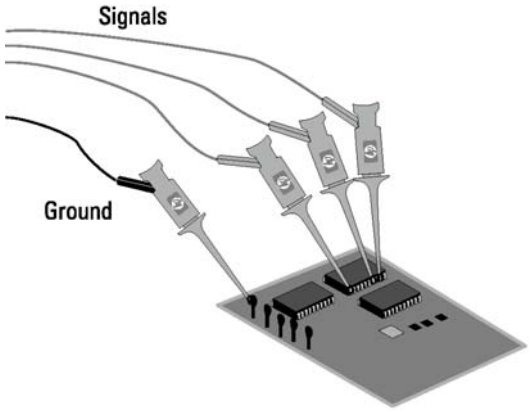

Figure 2 - Micrograbbers Attached To Circuit Under Test

The controls on the front panel of the logic analyzer can be divided into the following groups: softkeys and channel, horizontal, trigger, storage and general controls.

Softkeys are located at the bottom on the display and are used in conjunction with other controls. A legend will appear at the bottom of the display above each softkey describing its function depending on what other controls are in use.

Channel controls are used to select which channels will be displayed. Turn the Channel Select knob to position the desired channel on the display. You can assign a label instead of the channel name by pressing the label button and entering a name. The on/off button is used to add or remove a selected channel to or from the display. The position knob is used to move the position of a selected channel up or down with respect to the other display channels. The label button is used in conjunction with softkeys to label different channels with signal names.

Horizontal controls adjust the time scale and a delay from the trigger point to the display. The time/div knob controls the time scale. Turning counterclockwise lengthens the scale up to a maximum of 1 second per division while turning it clockwise shortens it to a minimum of 5ns/division. The trigger time of each trace is shown at the center of the display with an equal time before and after the trigger. The delay knob can be used to shift where the center point is displayed. This is used to scroll the time axis and display output before and after the trigger.

Trigger controls select how the logic analyzer captures data. Triggers can be specified in three ways. When the Edge button is pressed the softkeys allow you to select a channel and an edge type either rising↑ or falling↓ or glitch↕. This is similar to oscilloscope triggering. When the Pattern button is pressed the softkeys allow you to specify a multiple bit pattern. Each displayed input can be specified as a high, low or don't care value using the softkeys. Any time the inputs match this condition the logic analyzer is triggered. This is especially useful when debugging complex sequential circuits. The Adv button allows the specification of more advanced triggers. The HP 56420A manual describes these in detail.

Storage controls determine how data is collected and stored. The Run/Stop key is used to turn the collection of data on (Run) or off (Stop). Pressing the Run button once causes

the logic analyzer to continuously wait for a trigger and display data each time a trigger is encountered. Pressing it a second time stops this process. The Single key waits for a trigger condition once and display the result. This is useful when you want to see what happens in response to a single trigger event rather than repeated triggers. The Auto-Store button places the logic analyzer into a mode that displays values for previous traces at half brightness while the current trace is displayed at full brightness. This can be used to see what happens over multiple occurring events.

General controls are used to set up what is displayed. You can modify the display and measure time between events. The Measure Time button allows you to measure time between events. The Save/Recall buttons work with softkeys and allow you to save configurations and restore them. You will often uses these buttons in conjunction with the Default softkey to set the logic analyzer to display all channels. The Autoscale button is particularly useful because it will configure the logic analyzer to display all channels on which inputs are active and guesses an appropriate time scale. This is useful for quickly setting up the display, but it will not display channels on which there is no activity. On the bottom left of the display there is a row of dashes and/or arrows. An up-down arrow indicates activity on a particular probe channel whereas a dash does not.

The channel inputs include the probe connector and Logic Levels button. This button allows you to specify which logic family you will be debugging. This should be kept to the default value key TTL, which is the logic family we are using in this course.

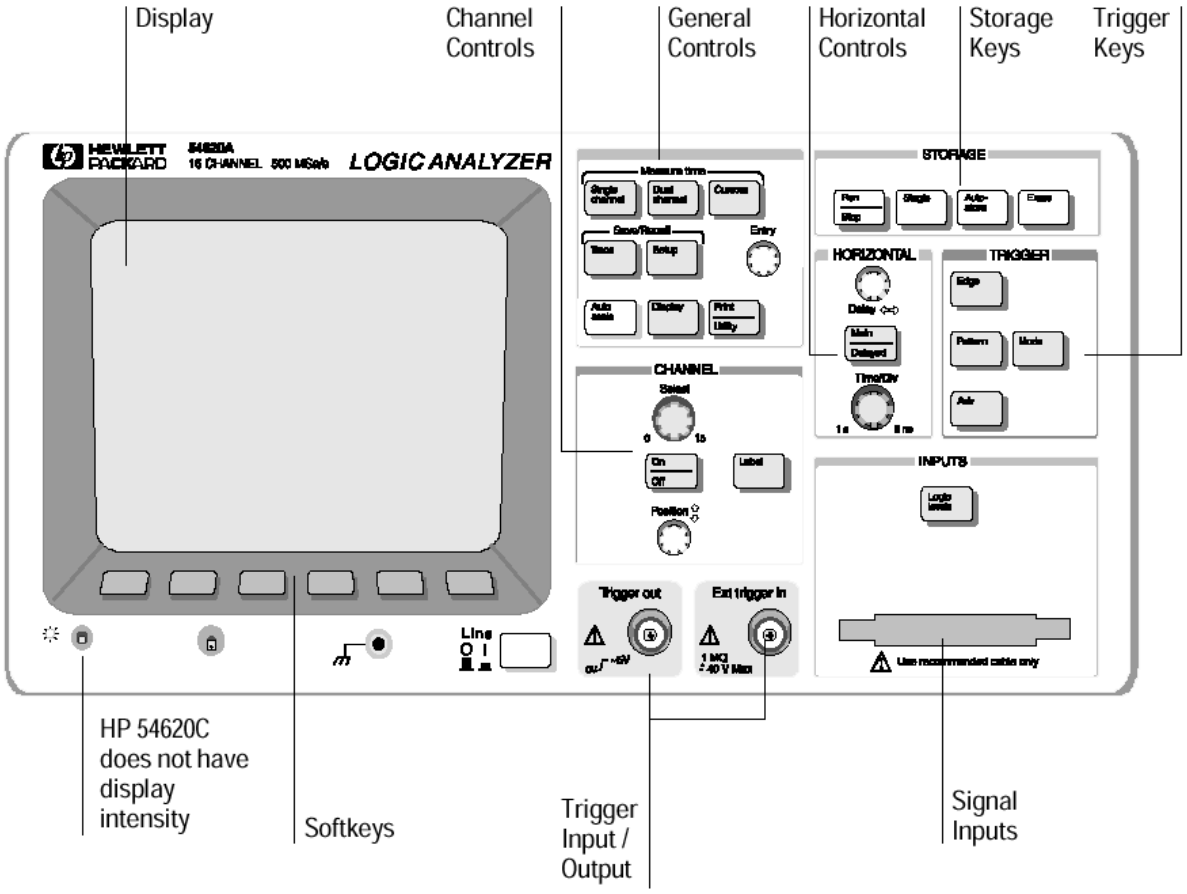

Figure 3 - Front Panel Controls

Pre-Lab

Before coming to lab you should have prepared a schematic for your design. You should be familiar with the pinouts of the integrated circuits you are using in your design and the front panel of the Sanper unit and its expansion interface.

In The Lab

In this lab you are to design an SRAM circuit to interface with Sanper. To assist in debugging your circuits, you will use the logic analyzer to explore the interface signals. You should probe the appropriate address bits; the upper and lower data strobes, read/write and data acknowledge signals as well as any others that may assist in debugging your particular design.

1. To start debugging your circuit you will first have to attach the necessary signal probes.

2. First attach the black ground probe to an easily accessible ground wire.

3. Then you should first start with the clock signal. Looking at the Sanper interface panel you should locate Clock and insert a wire into the breadboard. Then connect a micrograbber to the channel 0 probe and attach it to a clock wire.

4. You may now wish to turn on the Sanper unit and set the logic analyzer to trigger on the clock signal. Set the trigger to Edge and using the channel knob choose channel 0. Using the softkeys select the rising edge. You now have set you trigger.

5. Press Run to start triggering if the logic analyzer is not already doing so.

6. You may have to adjust the time/division knob to correctly observe the clock waveform. Notice what frequency it is.

7. After examining the clock waveform and exploring some of the logic analyzer's display features we will now connect more signals. However we will turn off the Sanper unit.

8. Using the rest of the probes we may now connect each of them in a similar manner to the UDS, LDS, DTACK and necessary Address bits.

9. Change the trigger from the clock to DTACK. We can do this by choosing to edge trigger on the DTACK probe. Since DTACK is a negative logic signal we should trigger on its negative edge instead. We can choose the negative edge by selecting the appropriate softkey. We can then set the logic analyzer to run and trigger whenever a negative edge DTACK transition is detected.

We could also trigger on other signals that we have connected to the analyzer. Using the logic analyzer we can test for a variety of conditions and watch how our circuit responds to any given stimulus. A sample waveform is shown in Figure 4.

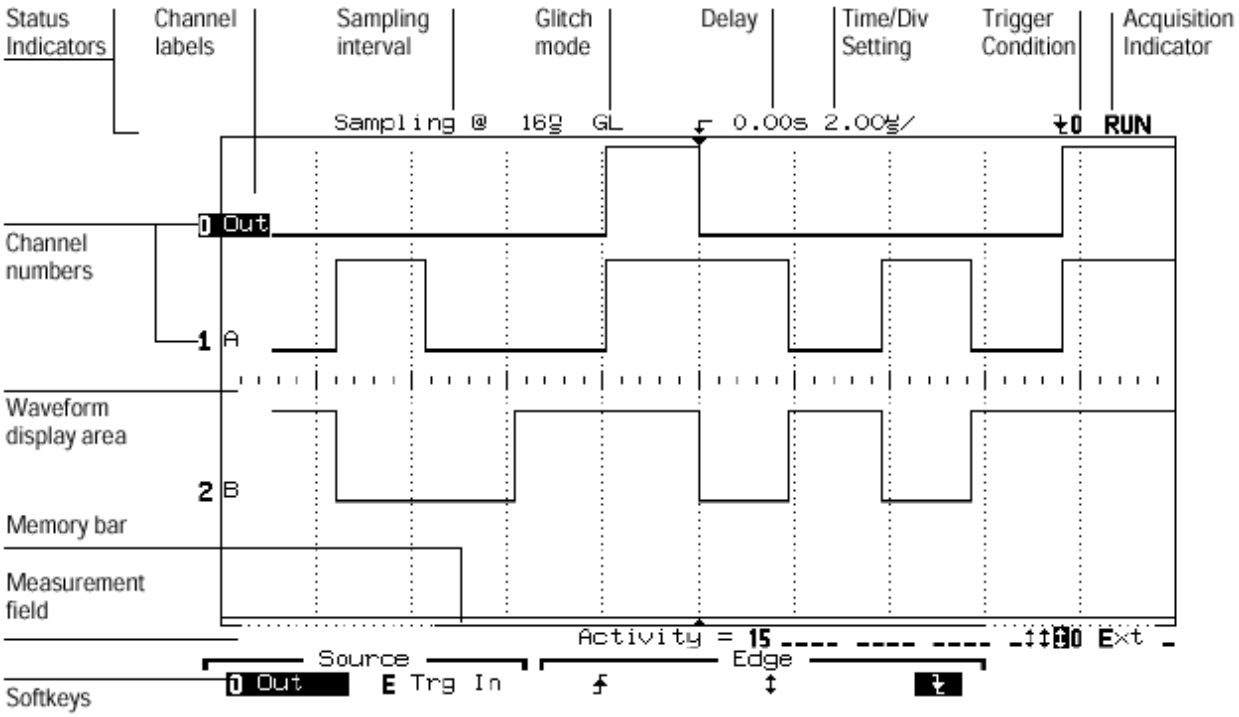

Figure 4 - Logic Traces

Conclusion

A Logic analyzer is a powerful debugging tool. However they are not a substitute for careful design and circuit construction. During the debugging process keep in mind that you are trying to isolate some problems they keep the circuit from working properly. This can either be a design or construction error. When starting with a faulty circuit, your job is to isolate where the fault occurs and determine how to fix it once it is isolated. In the following labs you'll have the opportunity to do this further.